FLEX I/O Isolated Analog Modules

Catalog Numbers 1794-IF4I, 1794-OF4I, 1794-IF2XOF2I, 1794-IF4IXT, 1794-IF4ICFXT, 1794-OF4IXT

Allen-Bradley
by ROCKWELL AUTOMATION

User Manual

Original Instructions

Important User Information

Read this document and the documents listed in the additional resources section about installation, configuration, and operation of this equipment before you install, configure, operate, or maintain this product. Users are required to familiarize themselves with installation and wiring instructions in addition to requirements of all applicable codes, laws, and standards.

Activities including installation, adjustments, putting into service, use, assembly, disassembly, and maintenance are required to be carried out by suitably trained personnel in accordance with applicable code of practice.

If this equipment is used in a manner not specified by the manufacturer, the protection provided by the equipment may be impaired.

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The examples and diagrams in this manual are included solely for illustrative purposes. Because of the many variables and requirements associated with any particular installation, Rockwell Automation, Inc. cannot assume responsibility or liability for actual use based on the examples and diagrams.

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Throughout this manual, when necessary, we use notes to make you aware of safety considerations.

WARNING: Identifies information about practices or circumstances that can cause an explosion in a hazardous environment, which may lead to personal injury or death, property damage, or economic loss.

ATTENTION: Identifies information about practices or circumstances that can lead to personal injury or death, property damage, or economic loss. Attentions help you identify a hazard, avoid a hazard, and recognize the consequence.

IMPORTANT Identifies information that is critical for successful application and understanding of the product.

These labels may also be on or inside the equipment to provide specific precautions.

SHOCK HAZARD: Labels may be on or inside the equipment, for example, a drive or motor, to alert people that dangerous voltage may be present.

BURN HAZARD: Labels may be on or inside the equipment, for example, a drive or motor, to alert people that surfaces may reach dangerous temperatures.

ARC FLASH HAZARD: Labels may be on or inside the equipment, for example, a motor control center, to alert people to potential Arc Flash. Arc Flash will cause severe injury or death. Wear proper Personal Protective Equipment (PPE). Follow ALL Regulatory requirements for safe work practices and for Personal Protective Equipment (PPE).

The following icon may appear in the text of this document.

Identifies information that is useful and can help to make a process easier to do or easier to understand.

Rockwell Automation recognizes that some of the terms that are currently used in our industry and in this publication are not in alignment with the movement toward inclusive language in technology. We are proactively collaborating with industry peers to find alternatives to such terms and making changes to our products and content. Please excuse the use of such terms in our content while we implement these changes.

Table of Contents

About This Publication

This manual describes how to install, wire, program, and troubleshoot your FLEX™ I/O isolated analog modules. This manual also shows you how to use the modules with Allen-Bradley® programmable controllers.

Download Firmware, AOP, EDS, and Other Files

Download firmware, associated files (such as AOP, EDS, and DTM), and access product release notes from the Product Compatibility and Download Center at rok.auto/pcdc.

Summary of Changes

This publication contains the following new or updated information. This list includes substantive updates only and is not intended to reflect all changes.

Topic	Page
Updated template	throughout
Added Inclusive Language Acknowledgement	Important User Information
Updated Additional Resources	5
Added section Power Requirements to About the FLEX I/O Isolated Analog Modules	9
Updated decimal input range for ±10V input value	35, 39, 53, 62, 68

Additional Resources

These documents contain additional information concerning related products from Rockwell Automation. You can view or download publications at rok.auto/literature.

Resource	Description
FLEX I/O and FLEX I/O-XT Selection Guide, publication 1794-SG001	Describes the FLEX I/O and FLEX I/O-XT™ system and provides specifications for the modules.
FLEX I/O Isolated Analog Output Module Installation Instructions, publication 1794-IN037	Information on how to install the FLEX I/O Isolated Analog Output Module.
FLEX I/O Isolated Analog Input Module Installation Instructions, publication 1794-IN038	Information on how to install the FLEX I/O Isolated Analog Input Module.
FLEX I/O Isolated Analog Input/Output Module Installation Instructions, publication 1794-IN039	Information on how to install the FLEX I/O Isolated Analog Input/Output Module.
FLEX I/O-XT Isolated Analog Input and Output Modules Installation Instructions, publication 1794-IN129	Information on how to install the FLEX I/O-XT Isolated Analog Input and Output Module.
FLEX I/O-XT Isolated Analog Input Module Installation Instructions, publication 1794-IN130	Information on how to install the FLEX I/O-XT Isolated Analog Input Module.
EtherNet/IP Network Devices User Manual, publication ENET-UM006	Describes how to configure and use EtherNet/IP™ devices to communicate on the EtherNet/IP network.
Ethernet Reference Manual, publication ENET-RM002	Describes basic Ethernet concepts, infrastructure components, and infrastructure features.
System Security Design Guidelines Reference Manual, publication SECURE-RM001	Provides guidance on how to conduct security assessments, implement Rockwell Automation products in a secure system, harden the control system, manage user access, and dispose of equipment.
UL Standards Listing for Industrial Control Products, publication CMPNTS-SR002	Assists original equipment manufacturers (OEMs) with construction of panels, to help ensure that they conform to the requirements of Underwriters Laboratories.
Industrial Components Preventive Maintenance, Enclosures, and Contact Ratings Specifications, publication IC-TD002	Provides a quick reference tool for Allen-Bradley industrial automation controls and assemblies.
Safety Guidelines for the Application, Installation, and Maintenance of Solid-state Control, publication SGI-1.1	Designed to harmonize with NEMA Standards Publication No. ICS 1.1-1987 and provides general guidelines for the application, installation, and maintenance of solid-state control in the form of individual devices or packaged assemblies incorporating solid-state components.
Industrial Automation Wiring and Grounding Guidelines, publication 1770-4.1	Provides general guidelines for installing a Rockwell Automation industrial system.
Product Selection and Configuration webpage, rok.auto/systemtools	Helps configure complete, valid catalog numbers and build complete quotes based on detailed product information.
Product Certifications website, rok.auto/certifications	Provides declarations of conformity, certificates, and other certification details.

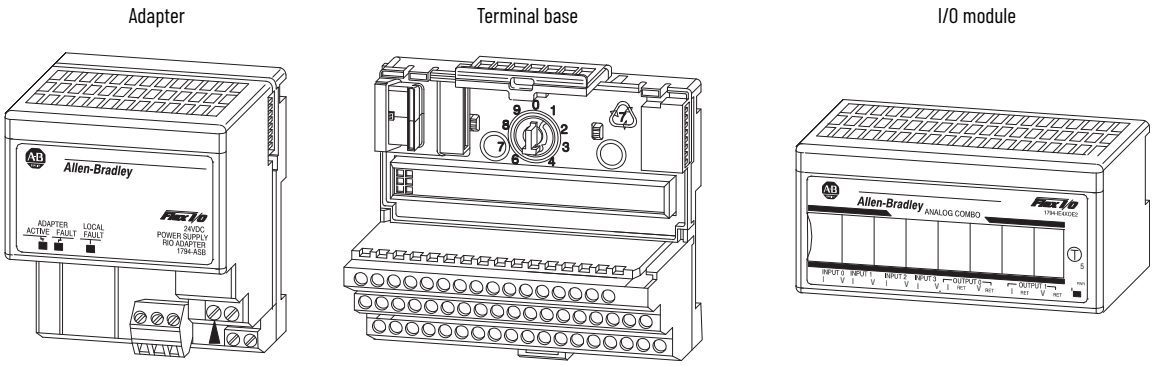
Notes:

About the FLEX I/O Isolated Analog Modules

The FLEX I/O System

FLEX I/O is a small, modular I/O system for distributed applications that performs all functions of rack-based I/O. The FLEX I/O system contains the following components that are shown in Figure 1.

Figure 1 - FLEX I/O System



- Adapter/power supply – Powers the internal logic for as many as eight I/O modules
- Terminal base – Contains a terminal strip to terminate wiring for two-wire or three-wire devices
- I/O module – Contains the bus interface and circuitry that is needed to perform specific functions that are related to your application

Types of FLEX I/O Modules

We describe the following FLEX I/O analog modules in this user manual.

Catalog Number	Voltage	Inputs	Outputs	Description
1794-IF4I	24V DC	4	—	Analog – 4 inputs, isolated
1794-OF4I	24V DC	—	4	Analog – 4 outputs, isolated
1794-IF2XOF2I	24V DC	2	2	Analog – 2 inputs, isolated and 2 outputs, isolated

FLEX I/O analog input, output, and combination modules are block transfer modules that interface analog signals with any Allen-Bradley programmable controllers that have block transfer capability. Block transfer programming moves input from the module's memory to a designated area in the processor data table, and output data words from a designated area in the processor data table to the module's memory. Block transfer programming also moves configuration words from the processor data table to module memory.

The analog modules have selectable ranges as shown in the following table.

Selectable Ranges for FLEX I/O Analog Modules

Input Values	Data Format	Underrange/Overrange
4...20 mA	Signed 2's complement	4% Underrange, 4% Overrange
±10V	Signed 2's complement	2% Underrange, 2% Overrange
±5V	Signed 2's complement	4% Underrange, 4% Overrange
0...20 mA	Signed 2's complement %	0% Underrange, 4% Overrange
4...20 mA	Signed 2's complement %	4% Underrange, 4% Overrange
0...10V	Signed 2's complement %	0% Underrange, 2% Overrange
±10V	Signed 2's complement %	2% Underrange, 2% Overrange
0...20 mA	Binary	0% Underrange, 4% Overrange

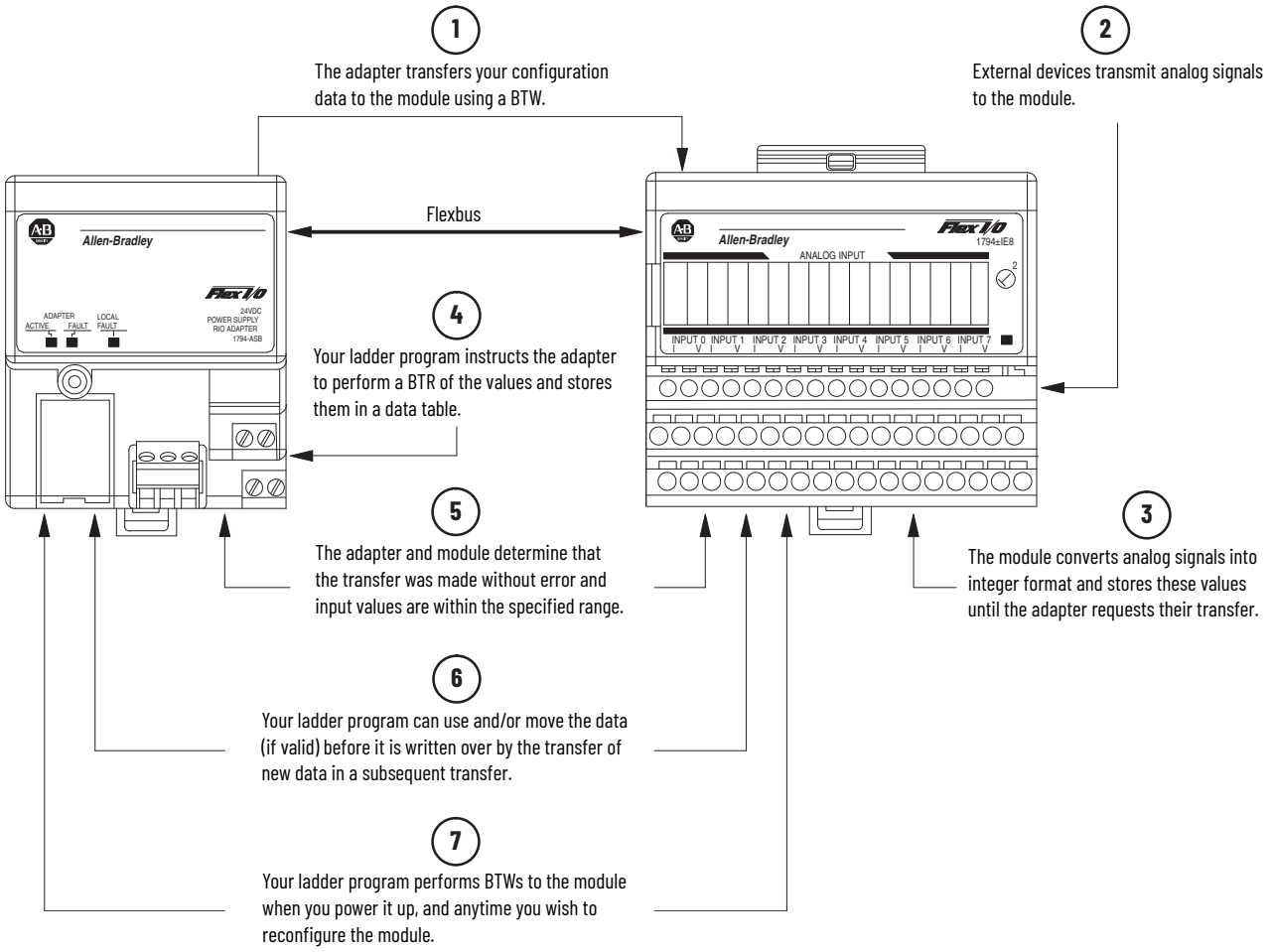
Selectable Ranges for FLEX I/O Analog Modules (Continued)

Input Values	Data Format	Underrange/Overrange
4...20 mA	Binary	4% Underrange, 4% Overrange
0...10V	Binary	0% Underrange, 2% Overrange
0...5V	Binary	0% Underrange, 4% Overrange
0...20 mA	Offset binary, 8000H = 0 mA	4% Underrange, 4% Overrange
4...20 mA	Offset binary, 8000H = 4 mA	4% Underrange, 4% Overrange
±10V	Offset binary, 8000H = 0V	2% Underrange, 2% Overrange
±5V	Offset binary, 8000H = 0V	4% Underrange, 4% Overrange

How FLEX I/O Analog Modules Communicate with Programmable Controllers

The adapter/power supply transfers data to the module (block-transfer write) and from the module (block-transfer read) using BTW and BTR instructions in your ladder diagram program. These instructions let the adapter obtain input values and status from the module, and let you send output values and establish the module's mode of operation. Figure 2 describes the communication process.

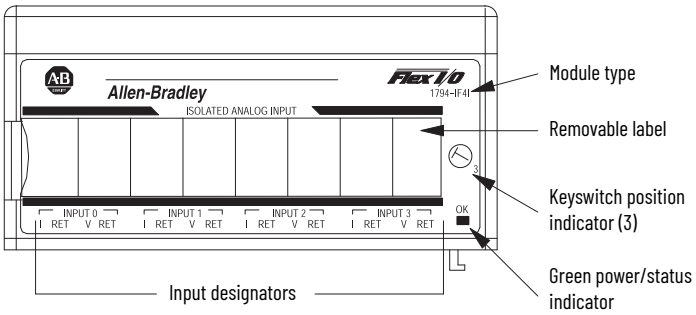
Figure 2 - Example of Communication Between an Adapter and an Analog Input Module



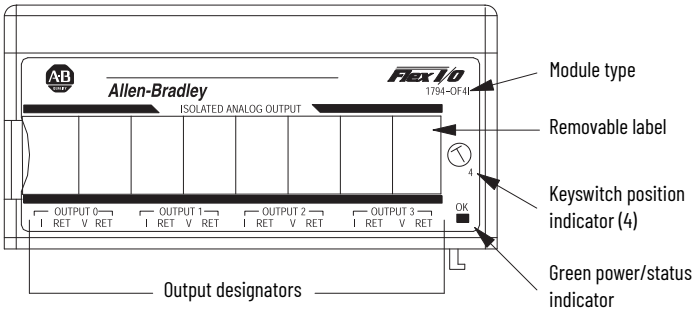
Features of Your Analog Modules

Each module has a unique label identifying its keyswitch position, wiring, and module type. A removable label provides space for writing individual designations per your application.

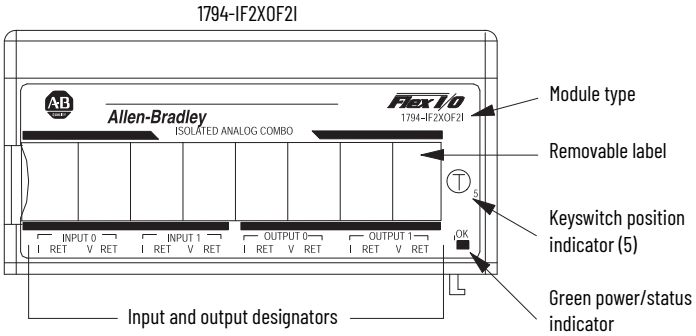
1794-IF4I



1794-OF4I



1794-IF2XOF2I



Power Requirements

The current draw through the terminal base determines the wiring of the terminal base unit. Verify that the current draw does not exceed 10 A.

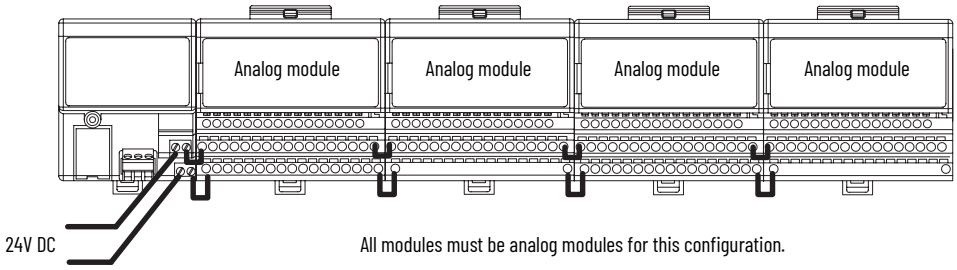
ATTENTION: Total current draw through the terminal base unit is limited to 10 A. Separate power connections may be necessary.

Methods of wiring the terminal base units are shown in the following illustration.

ATTENTION: Do not daisy chain power or ground from an analog terminal base unit to any AC or DC digital module terminal base unit.

Figure 3 - Terminal Base Wiring

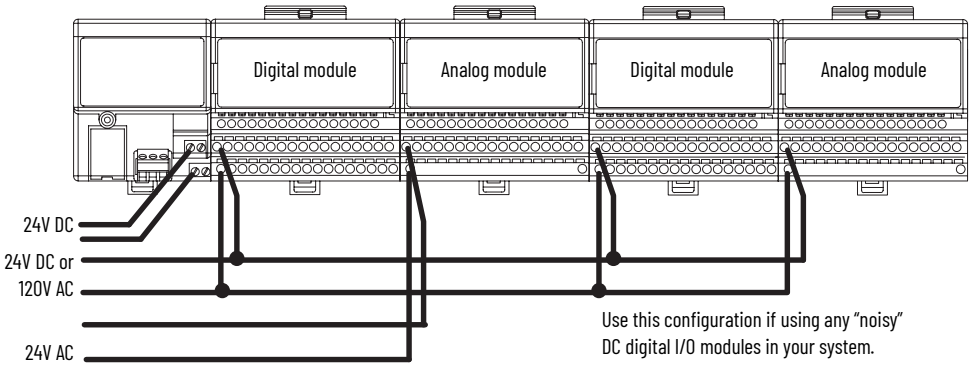
Daisy chaining



All modules must be analog modules for this configuration.

Wiring when total current draw is less than 10 A.

Individual

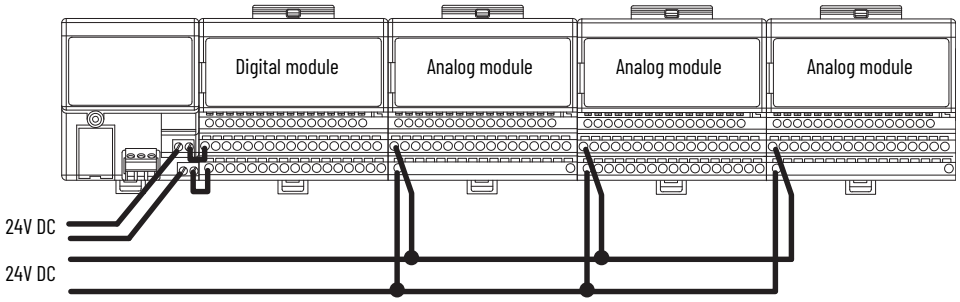


Use this configuration if using any "noisy" DC digital I/O modules in your system.

Analog module wiring is separate from digital module wiring.

Wiring when total current draw is greater than 10 A.

Combination



All modules that are powered by the same power supply must be analog modules in this configuration.

Total current draw through any base unit must not be greater than 10 A.

Module Programming

Block Transfer Programming

Your module communicates with the processor through bidirectional block transfers. This is the sequential operation of both read and write block transfer instructions.

A configuration block transfer write (BTW) is initiated when the analog module is first powered up, and then only when the programmer wants to enable or disable features of the module. The configuration BTW sets the bits, which enable the programmable features of the module, such as filters and signal ranges. Block transfer reads are performed to retrieve information from the module.

Block transfer read (BTR) programming moves status and data from the module to the processor's data table. The processor user program initiates the request to transfer data from the module to the processor. The transferred words contain module status, channel status, and input data from the module.

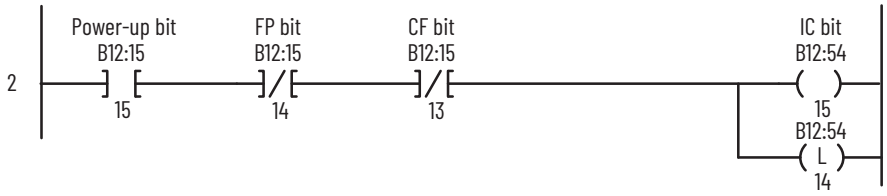
The following sample programs are minimum programs; all rungs and conditioning must be included in your application program. You can disable BTRs, or add interlocks to help prevent writes if desired. Do not delete any storage bits or interlocks that are included in the sample programs. If interlocks are removed, the program may not work properly.

Your program monitors the status bits, block transfer read, and block transfer write activity.

Configuration Rungs

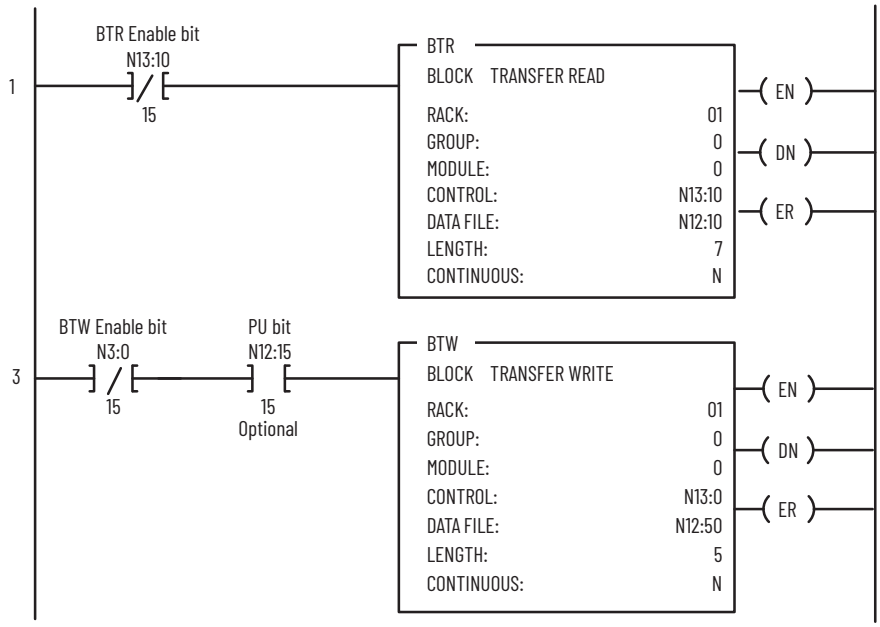
Example Configuration rungs

It is necessary to toggle the IC bit[(a)] (initiate configuration) for the isolated analog modules to accept configuration data. Once the configuration data has been properly configured, the following rung reconfigures the module (this example represents sizes for the 1794-IF4I module).



If there are rungs that already perform reads and writes to the module, no additional rungs are necessary. A simplified example of a BTR and BTW rung for 1794-IF4I follows (the 1794-OF4I is read length 6, write length 7; the 1794-IF2XOF2I is read length 7, write length 7):

(a) For systems that do not require ladder program control of configuration, set the TR bit (bit 13) to 1. See Chapter 3.



An XIC (--][--) instruction of the Power-up bit (PU) can be inserted to allow BTWs only when the module requires configuration (PU = 1).

Sample Programs for FLEX I/O Analog Modules

The following sample programs show you how to use your analog module efficiently when operating with a programmable controller. These programs show you how to:

- Configure the module.
- Read data from the module.
- Update the module's output channels (if used).

With Studio 5000 Logix Designer® application[(a)], simply read or write the tags provided. Studio 5000 Logix Designer application performs the transfer so an explicit block transfer is not required.

These programs illustrate the minimum programming that is required for communication to take place.

PLC-3 Programming

Block transfer instructions with the PLC-3® processor use one binary file in a data table section for module location and other related data. This is the block transfer control file. The block transfer data file stores data that you want transferred to your module (when programming a block transfer write) or from your module (when programming a block transfer read). The addresses of the block transfer data files are stored in the block transfer control file.

The same block transfer control file is used for both the read and write instructions for your module. Another block transfer control file is required for every module.

A sample program segment with block transfer instructions is shown in Figure 4, and described as follows.

(a) From version 21 onwards, RSLogix 5000® is known as Studio 5000 Logix Designer.

Figure 4 - PLC-3 Family Sample Program Structure for a 1794-IF4I Module

Program Action

At power-up in RUN mode, or when the processor is switched from PROG to RUN, the user program enables a block transfer read.

This rung toggles the Initiate Configuration bit from 0 to 1 to 0.

Then it initiates a block transfer write to configure the module if the power-up bit is set.
Thereafter, the program continuously performs read block transfers.
You must create the data file for the block transfers before you enter the block transfer instructions.

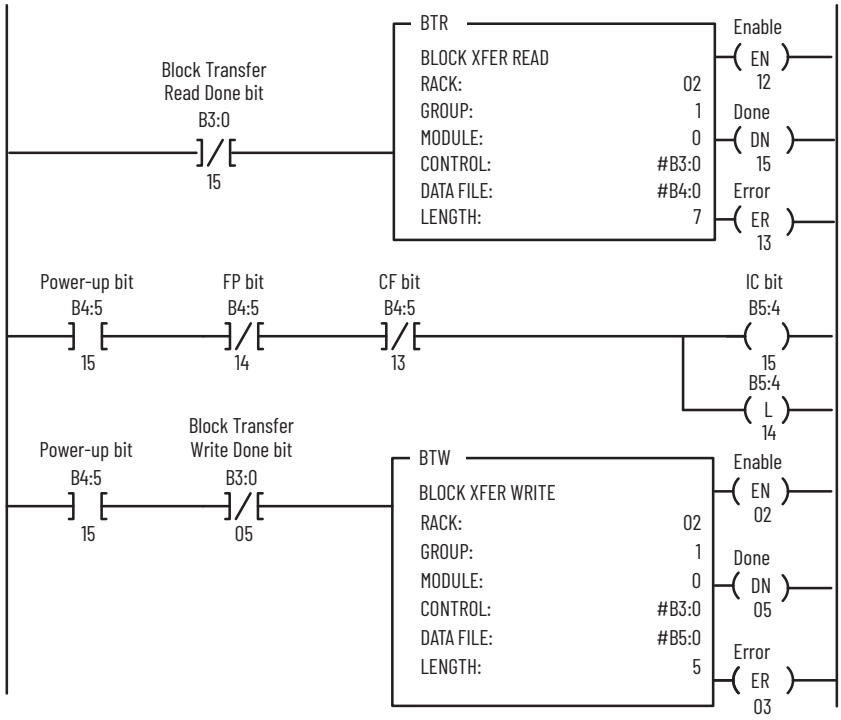


Figure 5 - PLC-3 Family Sample Program Structure for a 1794-IF2X0F2I Module

Program Action

At power-up in RUN mode, or when the processor is switched from PROG to RUN, the user program enables a block transfer read.

This rung toggles the Initiate Configuration bit from 0 to 1 to 0.

Then it initiates a block transfer write to configure the module and send data values.
Thereafter, the program continuously performs read block transfers and write block transfers.
You must create the data file for the block transfers before you enter the block transfer instructions.

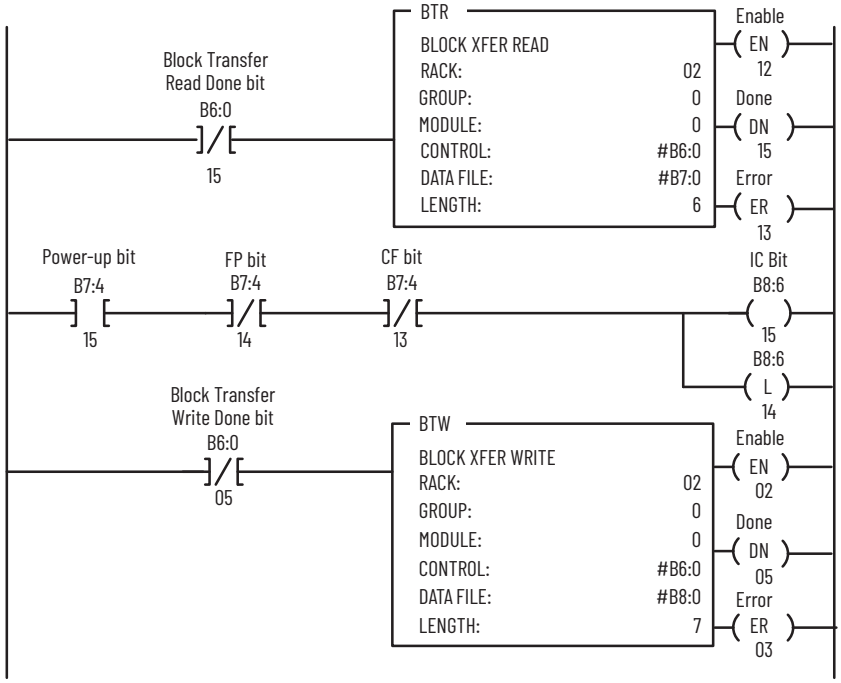


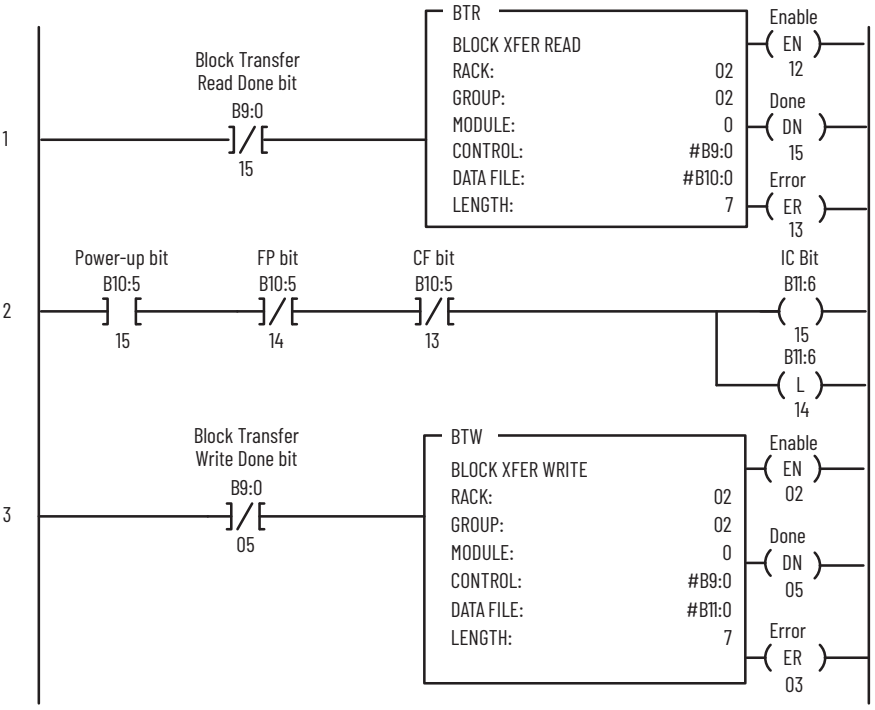
Figure 6 - PLC-3 Family Sample Program Structure for a 1794-OF4I Module

Program Action

At power-up in RUN mode, or when the processor is switched from PROG to RUN, the user program enables a block transfer read.

This rung toggles the Initiate Configuration bit from 0 to 1 to 0.

Then it initiates a block transfer write to configure the module and send data values.
Thereafter, the program continuously performs read block transfers and write block transfers.
You must create the data file for the block transfers before you enter the block transfer instructions.



PLC-5 Programming

The PLC-5® program is similar to the PLC-3 program with the following exceptions:

- Block transfer enable bits are used instead of done bits as the conditions on each rung.
- Separate block transfer control files are used for the block transfer instructions.

Figure 7 - PLC-5 Family Sample Program Structure for the 1794-IF4I

Program Action

At power-up in RUN mode, or when the processor is switched from PROG to RUN, the user program enables a block transfer read.

This rung toggles the Initiate Configuration bit from 0 to 1 to 0.

Then it initiates a block transfer write to configure the module if the power-up bit is set.
Thereafter, the program continuously performs read block transfers to configure the module.
The push button allows you to request a block transfer write manually.

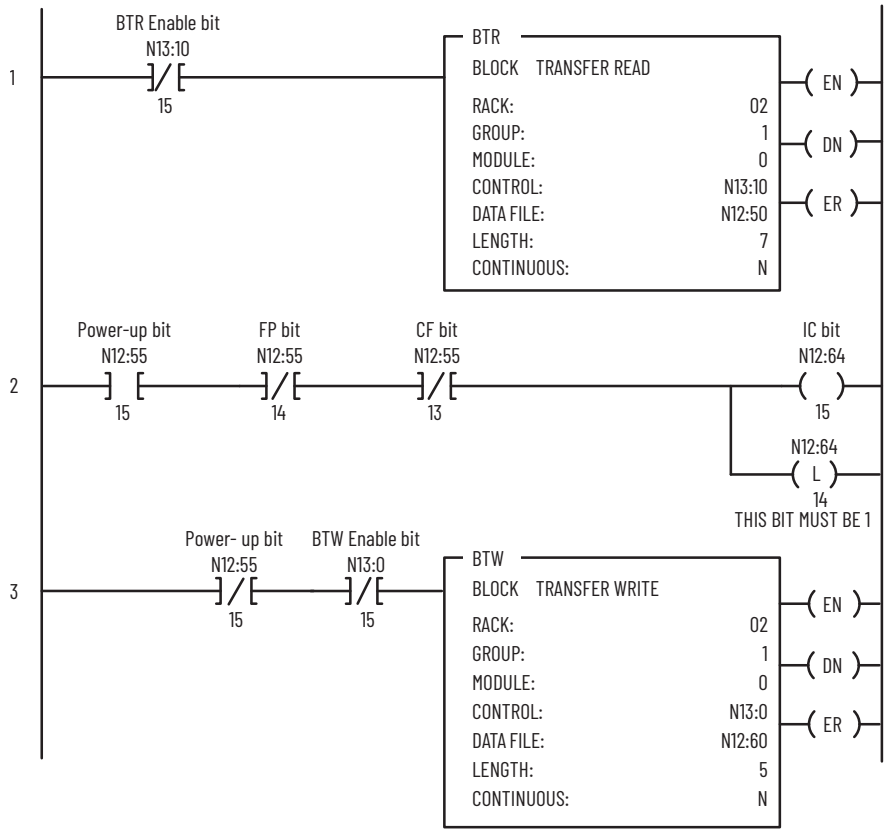


Figure 8 - PLC-5 Family Sample Program Structure for the 1794-OF4I

Program Action

At power-up in RUN mode, or when the processor is switched from PROG to RUN, the user program enables a block transfer read.

This rung toggles the Initiate Configuration bit from 0 to 1 to 0.

Then it initiates a block transfer write to configure the module and send data values.
Thereafter, the program continuously performs read block transfers and write block transfers.

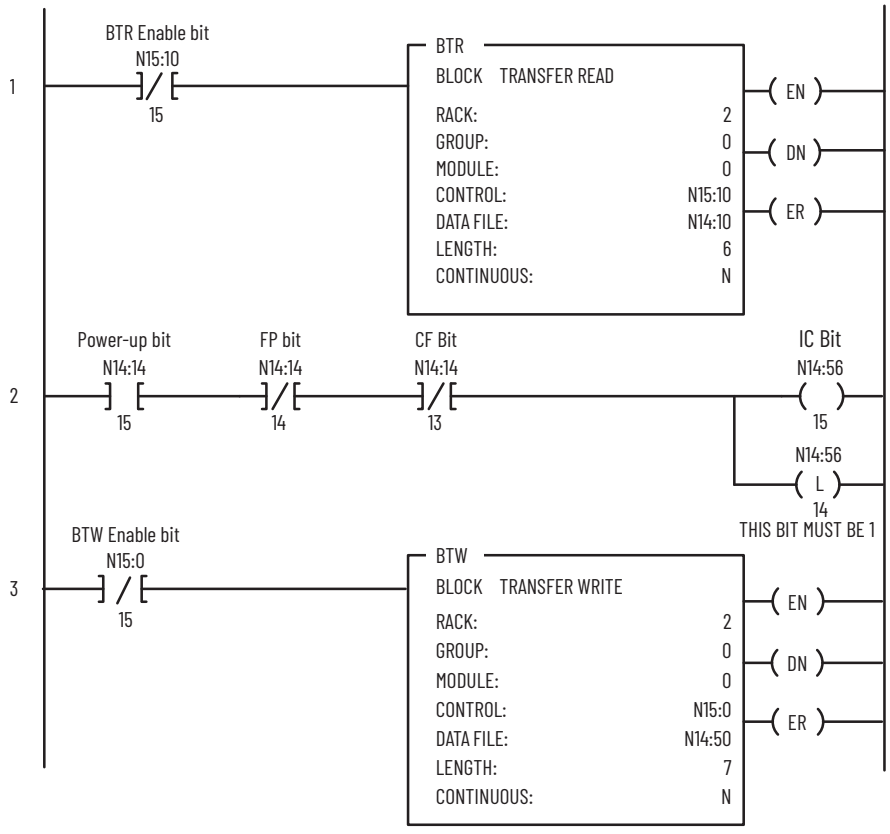


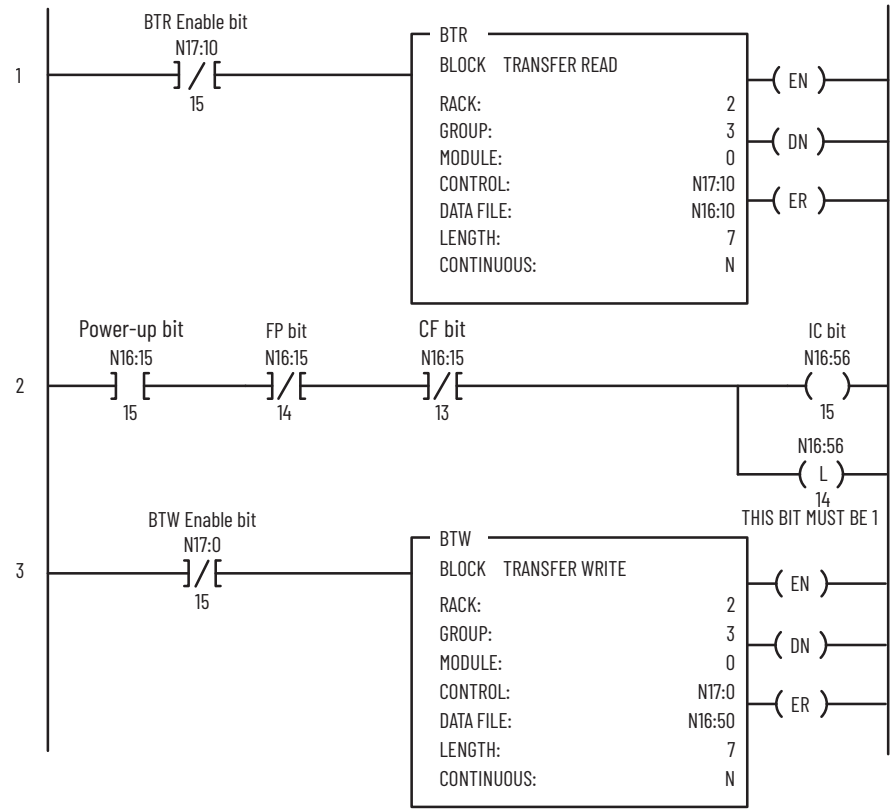
Figure 9 - PLC-5 Family Sample Program Structure for the 1794-IF2XOF2I

Program Action

At power-up in RUN mode, or when the processor is switched from PROG to RUN, the user program enables a block transfer read.

This rung toggles the Initiate Configuration bit from 0 to 1 to 0.

Then it initiates a block transfer write to configure the module and send data values.
Thereafter, the program continuously performs read block transfers and write block transfers.



PLC-2 Programming

The 1794 analog I/O modules are not recommended for use with PLC-2® family programmable controllers due to the number of digits needed for high resolution.

SLC Programming

The SLC™ 5/03, SLC 5/04, and SLC 5/05 programs (using the 1747-SN scanner) follow the same logic as the PLC-5 family programs in the previous examples. Differences occur in the implementation of block transfers due to the use of "M" files in the SLC™ system.

Configuration data for the FLEX I/O isolated analog modules and the 1747-SN scanner must be in place before executing the following programs. Chapter 4 contains information on the isolated analog module configurations.

For more information on using the 1747-SN scanner and block transfer programming, see the Remote I/O Scanner User Manual, publication 1747-UM013.

Figure 10 - SLC Programming for the 1794-OF4I Isolated Analog Output Module

Program Action

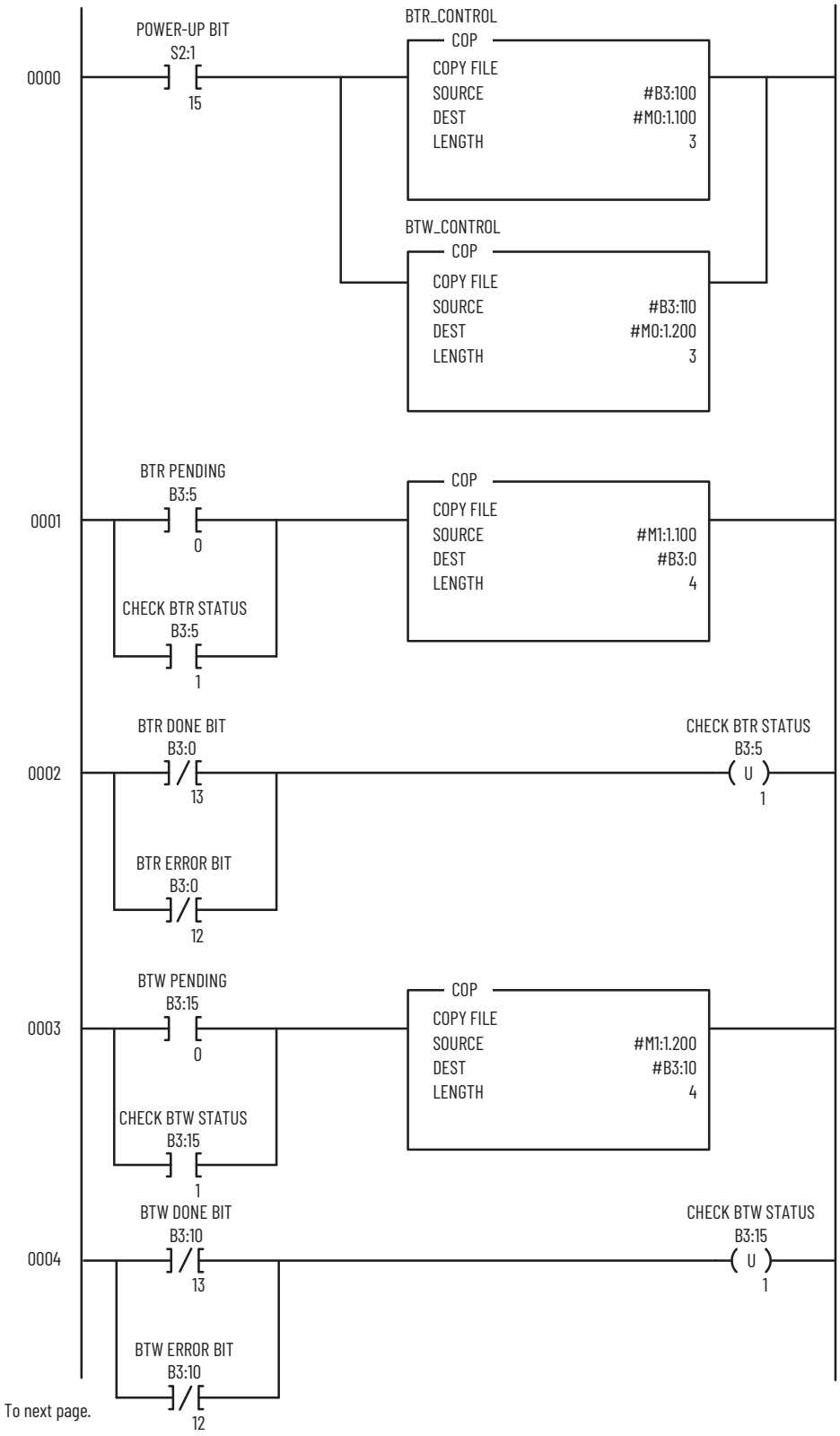
This rung configures the block transfer operation type, length, and RIO address at power-up. Bit B3:100/7 must be set to 1 to indicate a BTR and bit B3:110/7 must be 0 to indicate a BTW.

BTR status is copied to the B3:0 area when a BTR is in progress.

Unlatch the bit that continues to check the BTR status.

BTW status is copied to the B3:100 area when a BTW is in progress.

Unlatch the bit that continues to check the BTW status.

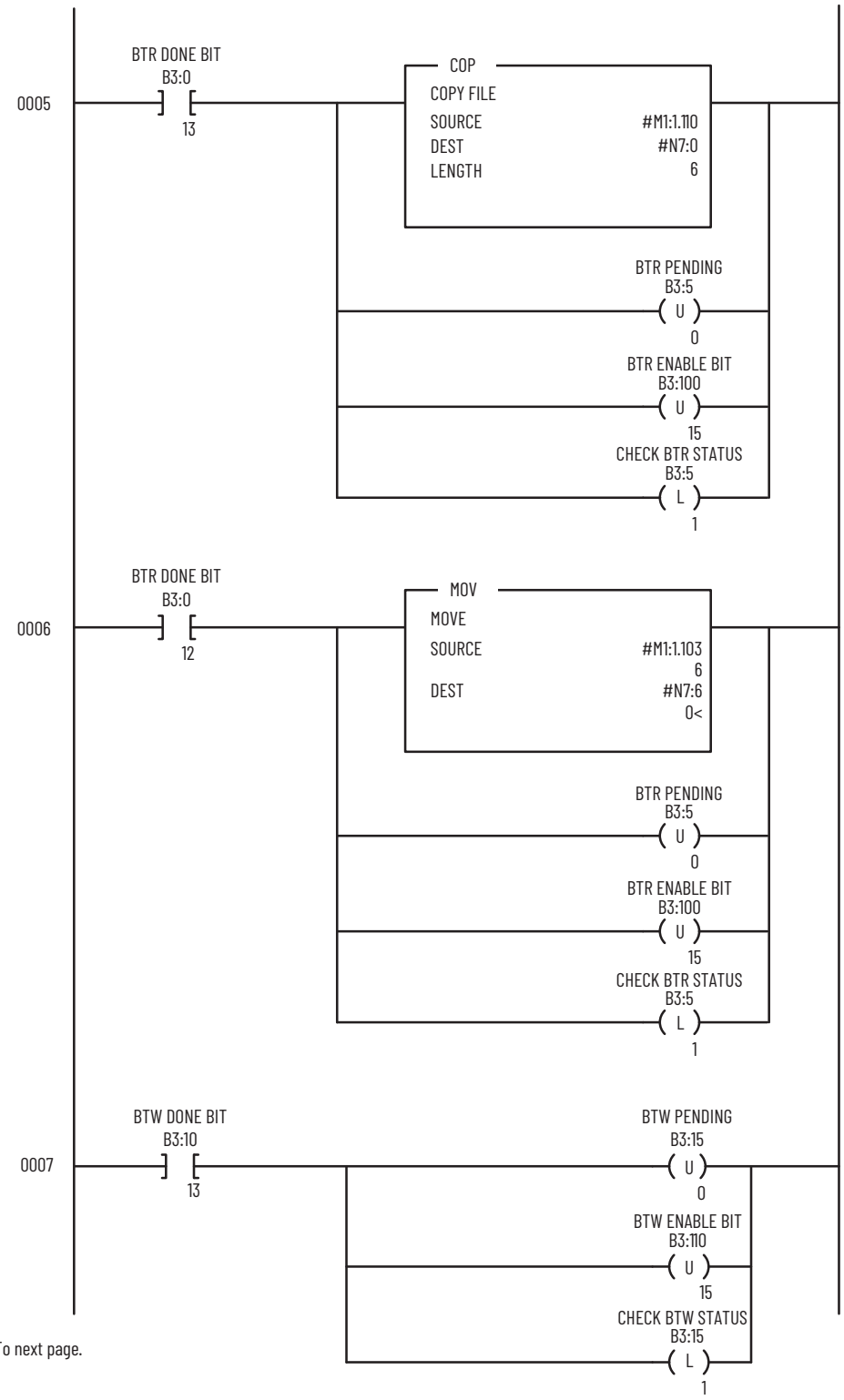


Program Action

This rung buffers the BTR data when a transfer is successfully completed.

This rung buffers the error code if a BTR is not successful.

This rung manipulates the flags for the BTW.



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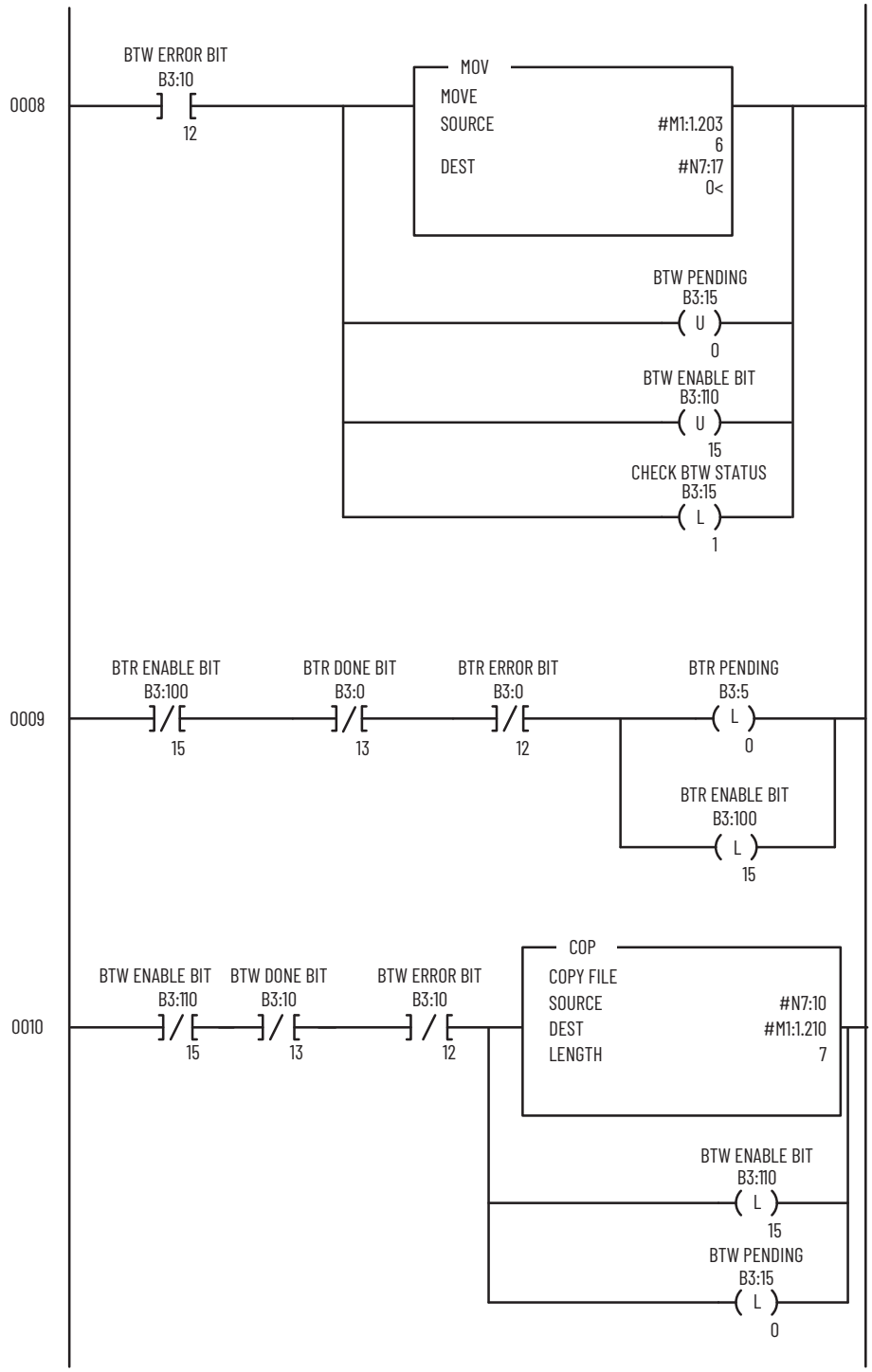
Program Action

This rung buffers the error code if a BTW is not successful.

This rung executes BTRs continuously.

This rung copies the write data to the M0 file and executes BTWs continuously. The configuration data for the FLEX module is placed in the write data.



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Program Action

This BTR control word is moved to the M0 file for the scanner.

This BTW control word is moved to the M0 file for the scanner.

This rung toggles the initiate configuration bit from 0 to 1 to 0.

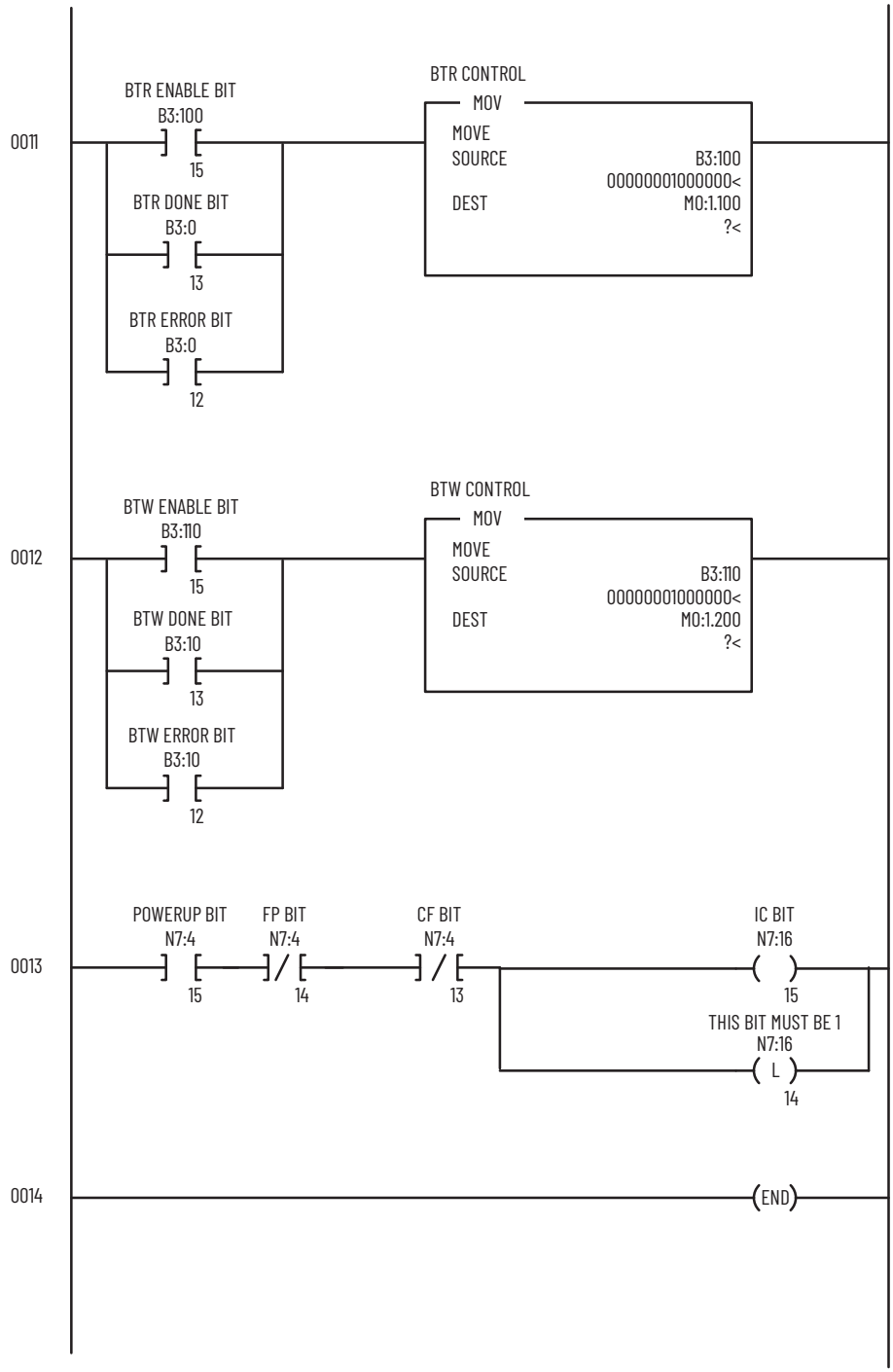


Figure 11 - SLC Programming for the 1794-IF4I Isolated Analog Input Module

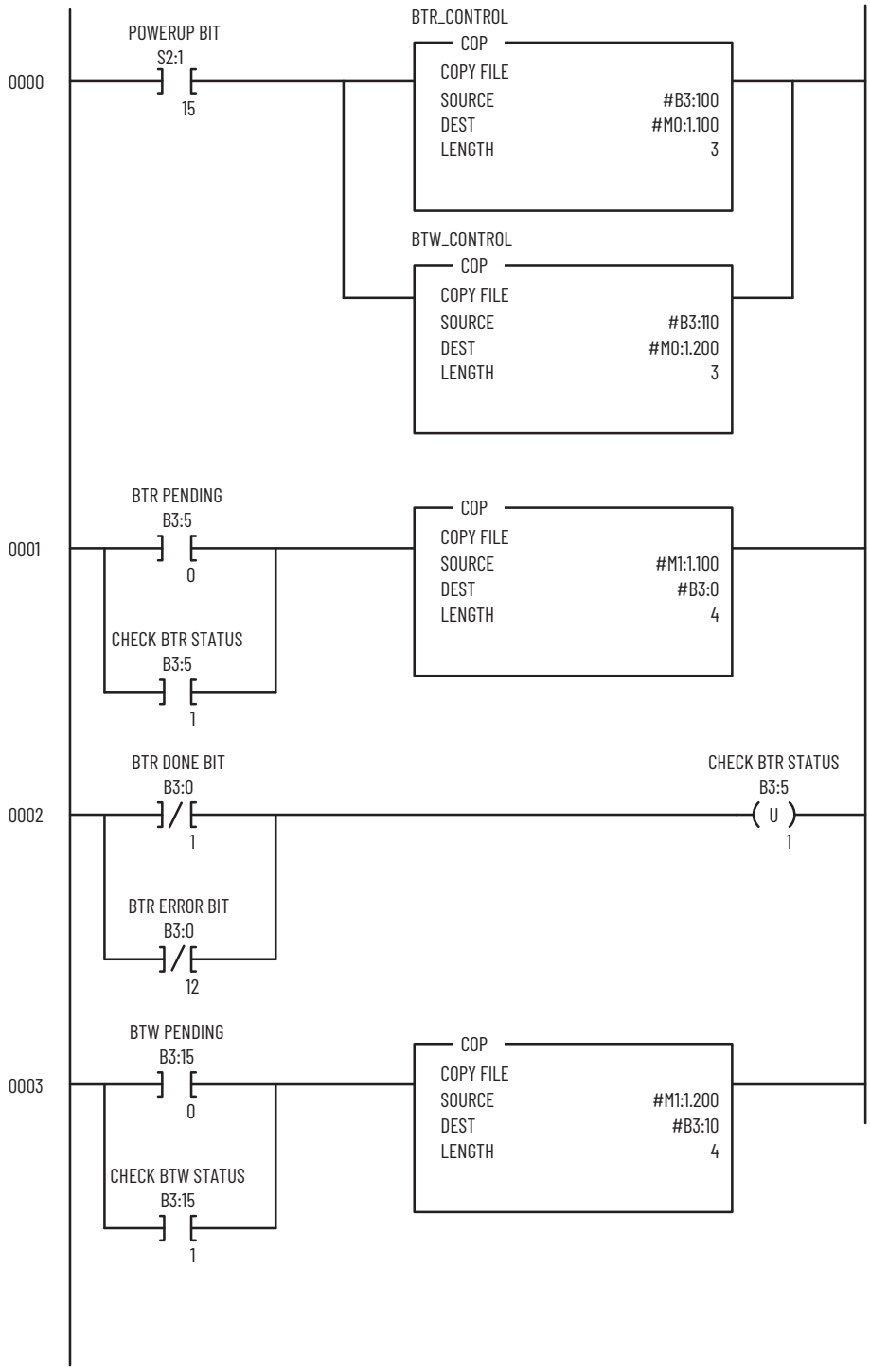
Program Action

This rung configures the block transfer operation type, length, and RIO address at power-up. Bit B3:100/7 must be set to 1 to indicate a BTR and bit B3:110/7 must be 0 to indicate a BTW.

BTR status is copied to the B3:0 area when a BTR is in progress.

Unlatch the bit that continues to check the BTR status.

BTW status is copied to the B3:100 area when a BTW is in progress.



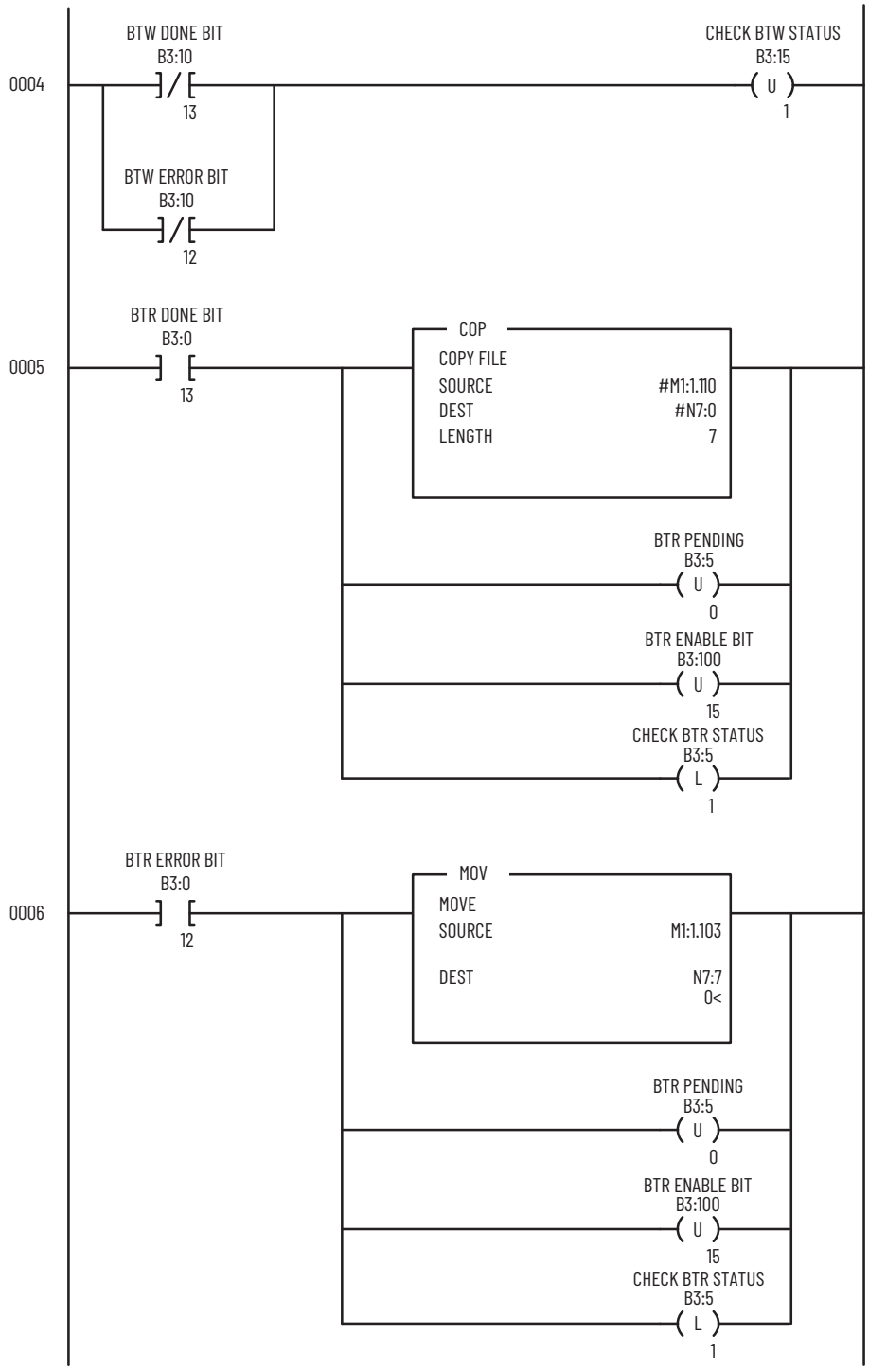
To next page.

Program Action

Unlatch the bit that continues to check the BTW status.

This rung buffers the BTR data when a transfer is successfully completed.

This rung buffers the error code if a BTR is not successful.



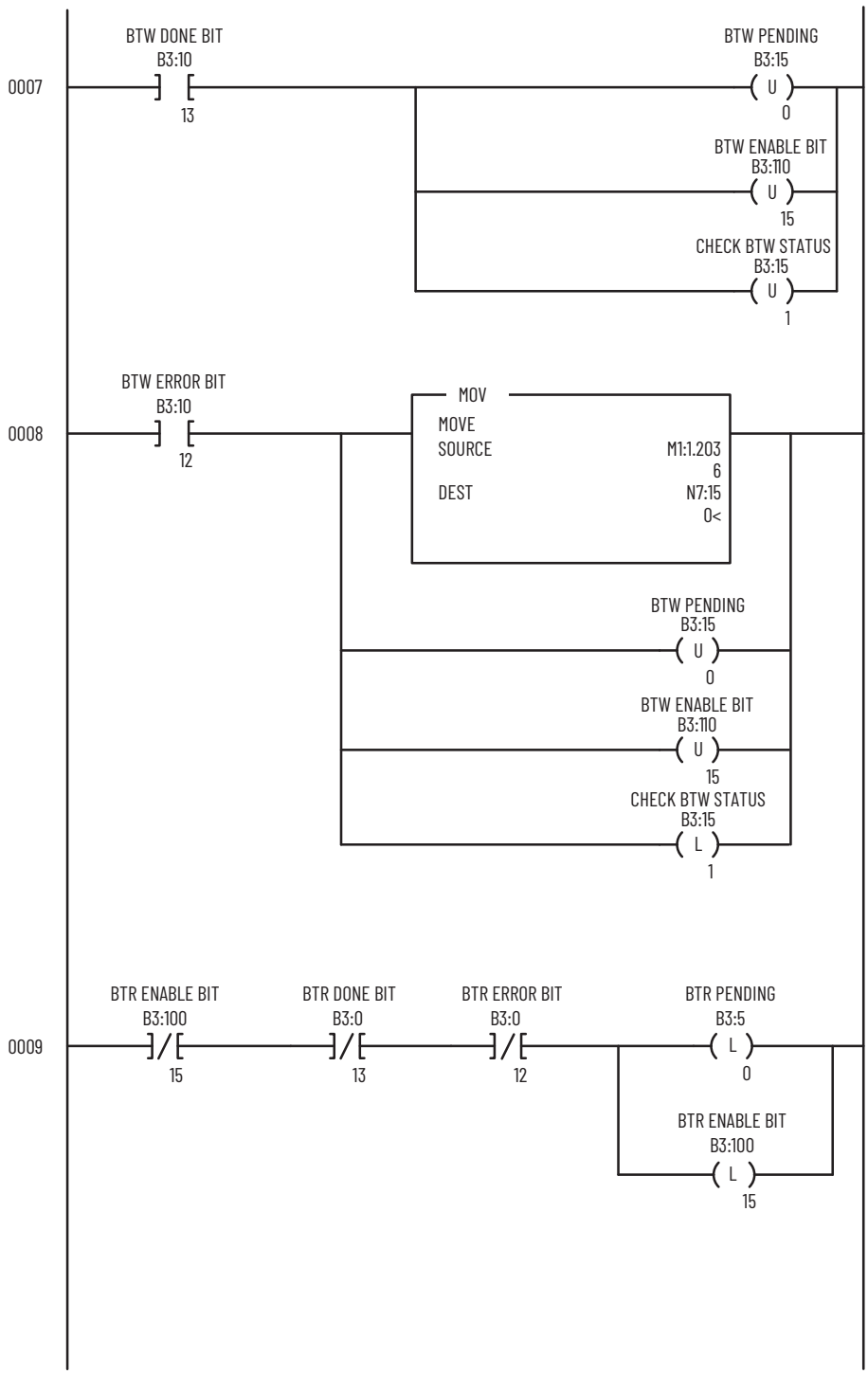
To next page.

Program Action

This rung manipulates the flags for the BTW.

This rung buffers the error code if a BTW is not successful.

This rung executes BTRs continuously.



To next page.

Program Action

This rung executes a BTW to configure the module when the power-up bit (PU) is set.

This BTR control word is moved to the M0 file for the scanner.

This BTW control word is moved to the M0 file for the scanner.

This rung toggles the initiate configuration bit from 0 to 1 to 0.

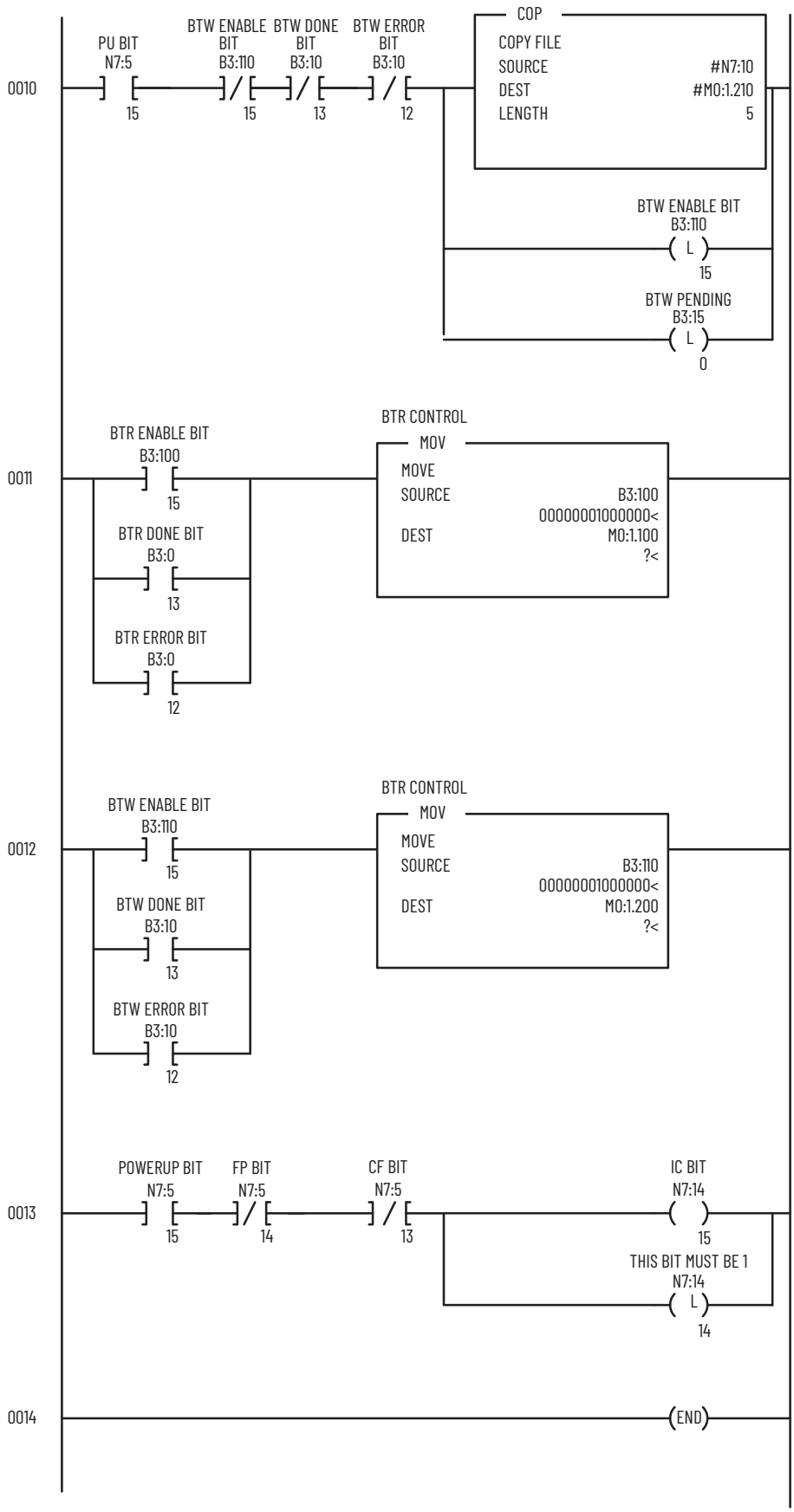


Figure 12 - SLC Programming for the 1794-IF2XOF2I Isolated Analog Input/Output Module

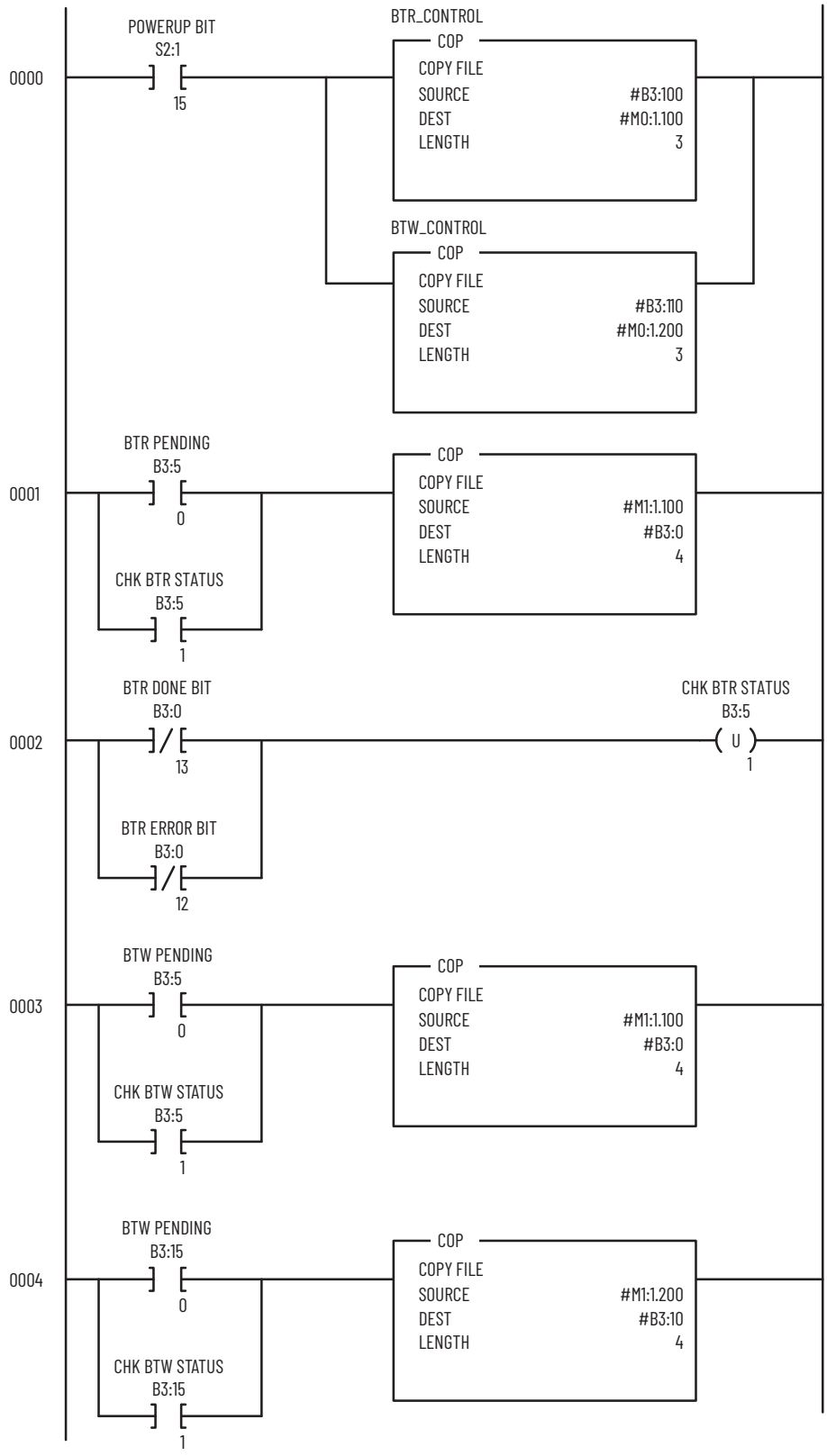
Program Action

This rung configures the block transfer operation type, length, and RIO address at power-up. Bit B3:100/7 must be set to 1 to indicate a BTR and bit B3:110/7 must be 0 to indicate a BTW.

Unlatch the bit that continues to check the BTR status.

BTW status is copied to the B3:100 area when a BTW is in progress.

This rung toggles the initiate configuration bit from 0 to 1 to 0.



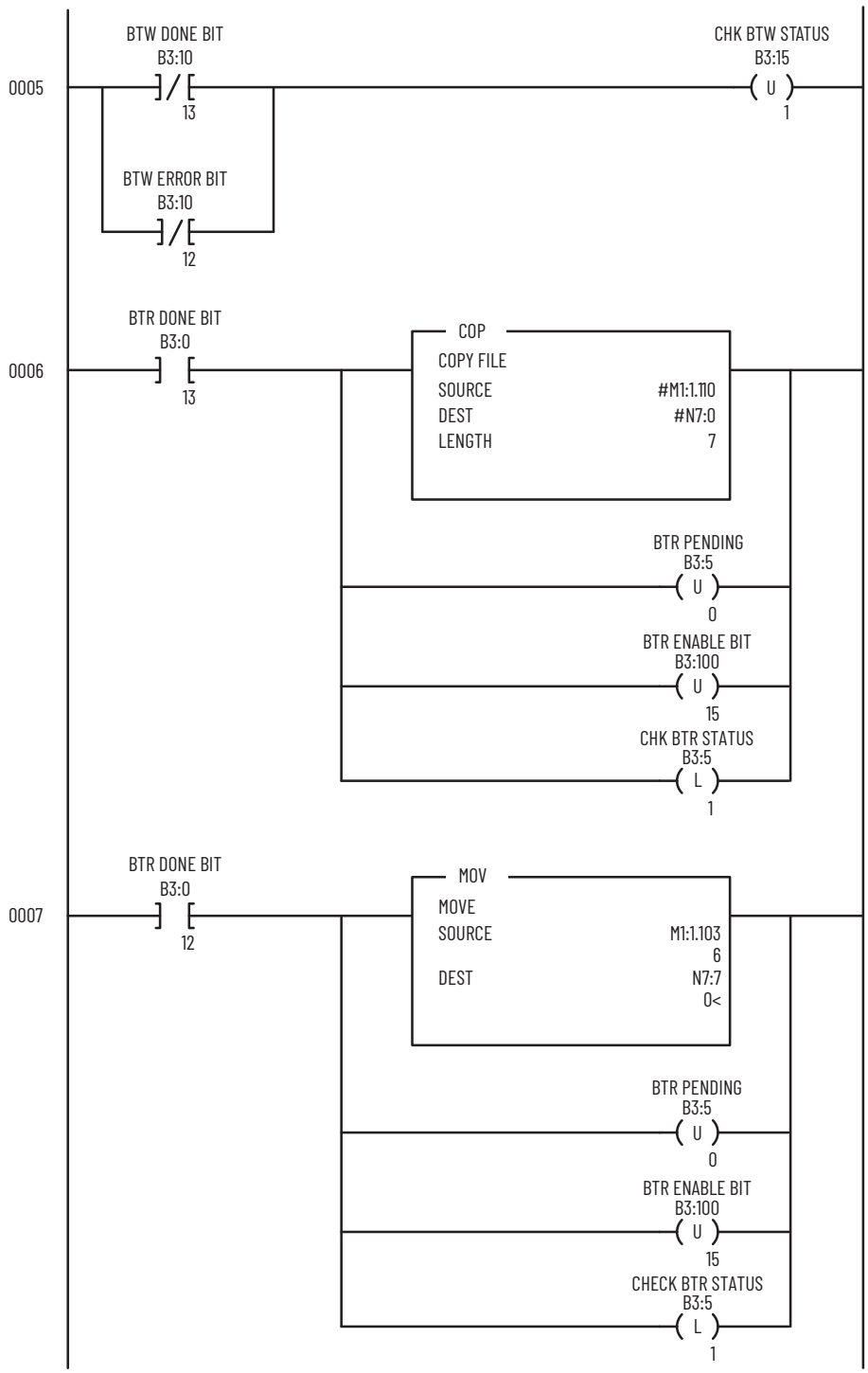
To next page.

Program Action

Unlatch the bit that continues to check the BTW status.

This rung buffers the BTR data when a transfer is successfully completed.

This rung buffers the error code if a BTR is not successful.



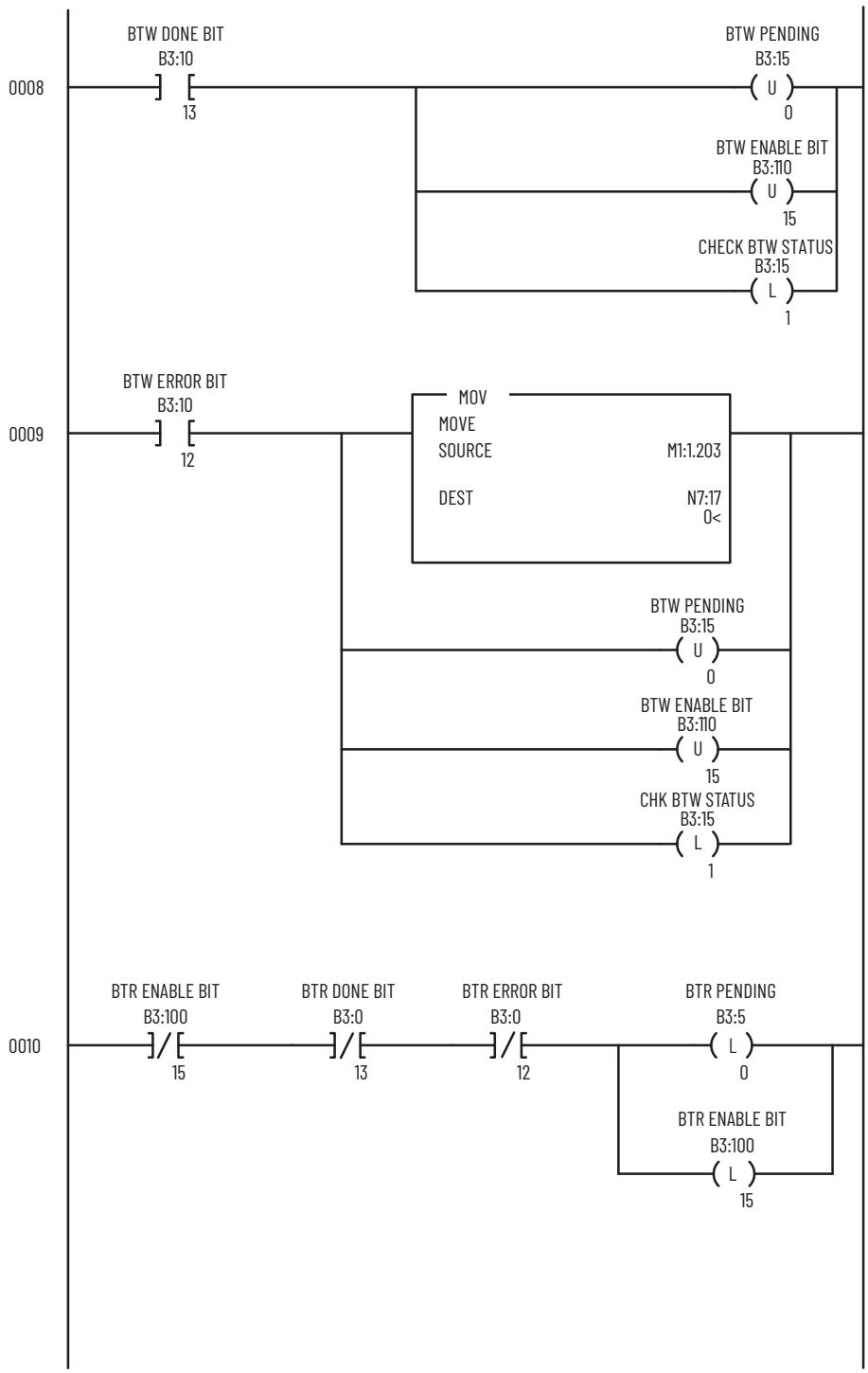
To next page.

Program Action

This rung manipulates the flags for the BTW.

This rung buffers the error code if a BTW is not successful.

This rung executes BTRs continuously.



To next page.

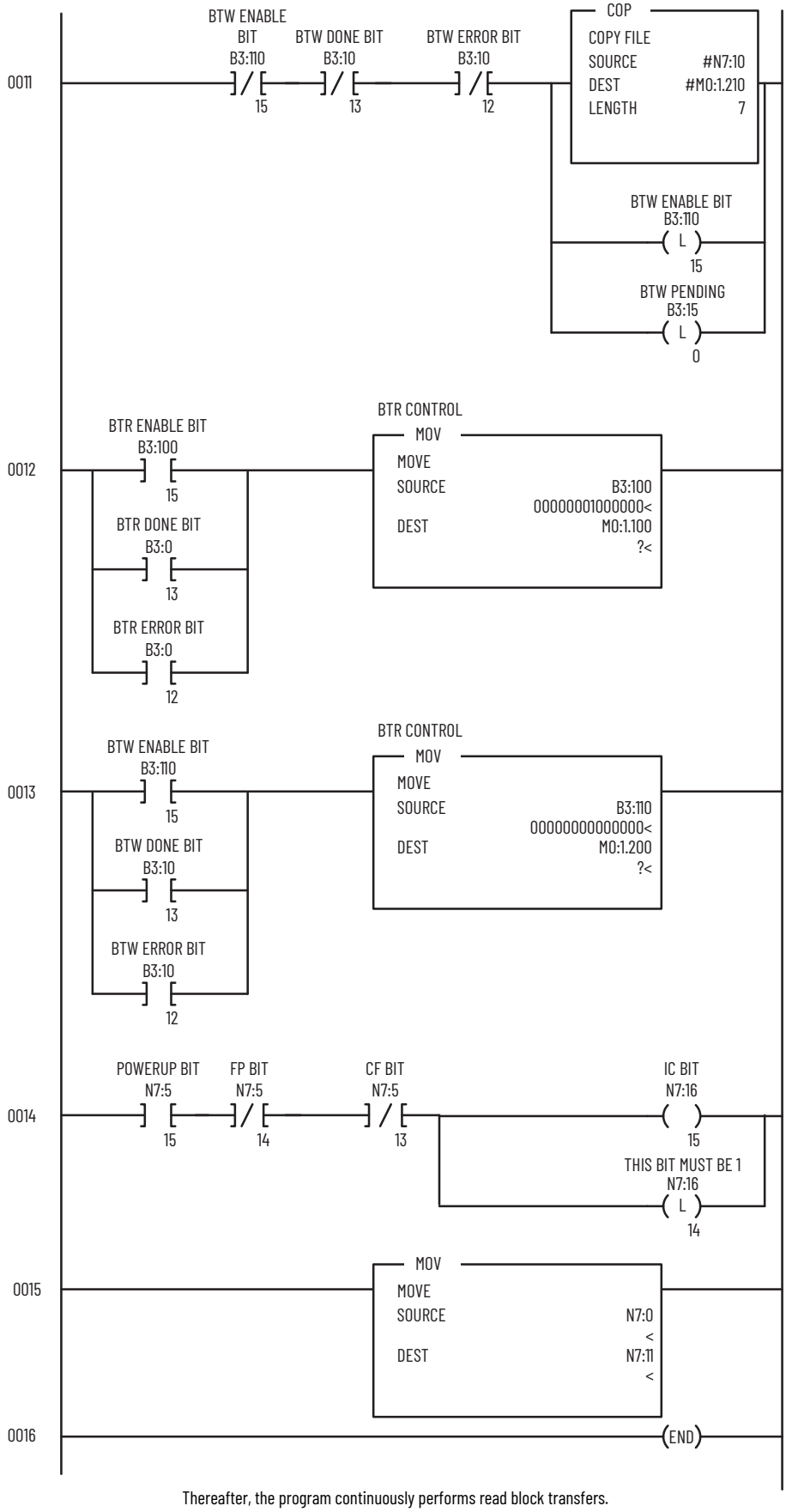
Program Action

This rung executes a BTW to configure the module when the power-up bit is set. The configuration data for the FLEX module is placed in the write data.

This BTR control word is moved to the M0 file for the scanner.

This BTW control word is moved to the M0 file for the scanner.

This rung toggles the initiate configuration bit from 0 to 1 to 0.



Thereafter, the program continuously performs read block transfers.

Write Configuration to and Reading Status from Your Module with a Remote I/O Adapter

Configure Your Analog Module

Because of the many analog devices available and the wide variety of possible configurations, you must configure your module to conform to the analog device and the specific application that you have chosen. The module is configured using a group of data table words that are transferred to the module using a block-transfer write instruction.

The software configurable features available are:

- Input/output range selection
- Data type (two's complement, two's complement percent, binary and offset binary)

PLC-5 family programmable controllers that use 6200 software programming tools can take advantage of the IOCONFIG utility to configure these modules. IOCONFIG uses menu-based screens for configuration without having to set individual bits in particular locations. See your 6200 software literature for details.

Logix 5000® family programmable controllers that use the Studio 5000 Logix Designer application can take advantage of the configuration GUI to configure these modules.

Range Selection

Individual input channels are configurable to operate with the following voltage or current ranges.

Table 1 - Range Selection

Input Channel Configuration		
Input Values	**Data Format**	**% Underrange/% Overrange**
Channel not configured		
4...20 mA	Signed 2's complement	4% Under; 4% Over
±10V	Signed 2's complement	2% Under; 2% Over
±5V	Signed 2's complement	4% Under; 4% Over
0...20 mA	Signed 2's complement %	0% Under; 4% Over
4...20 mA	Signed 2's complement %	4% Under; 4% Over
0...10V	Signed 2's complement %	0% Under; 2% Over
±10V	Signed 2's complement %	2% Under; 2% Over
0...20 mA	Binary	0% Under; 4% Over
0...10V	Binary	0% Under; 2% Over
0...5V	Binary	0% Under; 4% Over
0...20 mA	Offset binary, 8000 H = 0 mA	4% Under; 4% Over
4...20 mA	Offset binary, 8000 H = 4 mA	4% Under; 4% Over
±10V	Offset binary, 8000 H = 0V	2% Under; 2% Over
±5V	Offset binary, 8000 H = 0V	4% Under; 4% Over

You can select individual channel ranges using the designated words of the write block transfer instruction. See the Bit/Word description for your particular module for word and bit numbers.

Safe State Selection

You can select the analog values that your output module maintains if there is a network communication error. When a communication error clears the enable bit, the analog outputs automatically switch to the values set in the safe state analog words as defined by the safe state source bits. This allows you to select a reset to 0V/0 mA, or hold the outputs at their last state when using the remote I/O adapter on remote I/O. Additionally, safe state values can be setup using ControlNet®, DeviceNet®, or other network adapter.

Data Format

The input/output data that is exchanged between the module and the adapter is available in two's complement, two's complement percent, binary and offset binary (see Range Selection on page 29).

Real-time Sampling

Real-time sampling (RTS) provides data that is gathered at precise intervals for use by the processor. You set a word in the block-transfer write data file to enable RTS.

The real-time sample programmed interval is the time at which updated information is supplied to the processor. When set to "0" the module defaults to each channel's fastest update rate, which is dependent on the nominal range of the input and the filter setting set to "no low pass."

When the IT interrupt toggle bit is set (1), interleaving of module interrupts occurs, ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5 ms update rate are reduced to 5.0 ms. When reset (0), real-time sampling and filter features are enabled.

Table 2 - Real-time Sample Interval

Configuration	Nominal Range	Channel Update Rate (RTS = 0)(1)	Channel Update Rate (RTS and Filter = 0)(1) and IT = 1
1	4...20 mA	7.5 ms	5.0 ms
2	±10V	2.5 ms	2.5 ms
3	±5V	2.5 ms	2.5 ms
4	0...20 mA	7.5 ms	5.0 ms
5	4...20 mA	7.5 ms	5.0 ms
6	0...10V	5.0 ms	5.0 ms
7	±10V	5.0 ms	5.0 ms
8	0...20 mA	2.5 ms	2.5 ms
9	4...20V	7.5 ms	5.0 ms
A	0...10V	2.5 ms	2.5 ms
B	0...5V	2.5 ms	2.5 ms
C	0...20 mA	2.5 ms	2.5 ms
D	4...20 mA	7.5 ms	5.0 ms
E	±10V	2.5 ms	2.5 ms
F	±5V	2.5 ms	2.5 ms

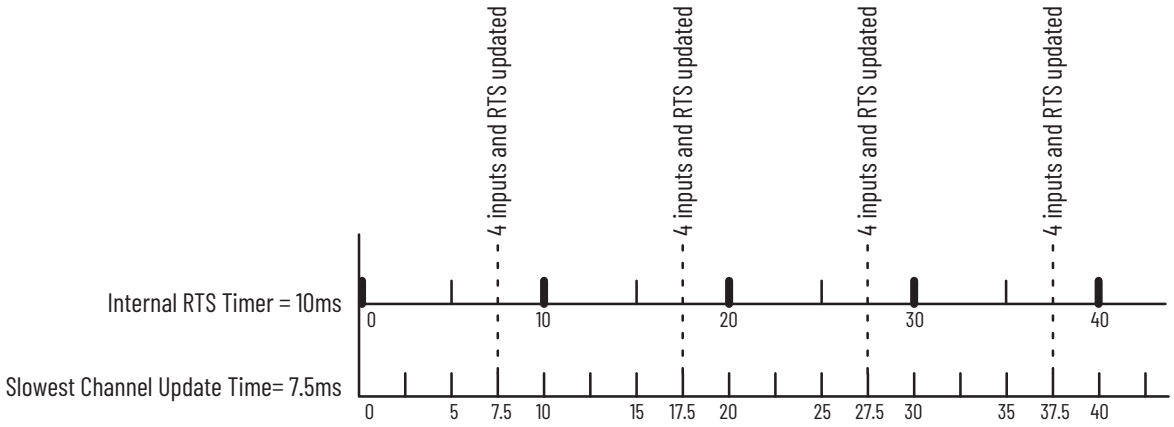
(1) Channel filter set to "no low pass".

The real-time sample interval can be set from 0 to 30s, in increments of 5 ms. Set the real-time sample interval in binary using 15 bits in the block-transfer write word.

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 3	0					Real-time Sample Programmed Intervals										

The individual channel update times determine how fast you can get new information collectively from the module. The module gathers the data from each input and makes it available to the processor. For example, if channel 0 is 2.5 ms, channel 1 is 5.0 ms, and channel 2 is 7.5 ms, and RTS = 0, each channel is updated at its stated rate. If RTS is set to 5 ms, only channels 0 and 1 are fast enough to be included in the real-time sample. To include channel 2 in your synchronous sample, you must set the RTS to 10 ms minimum. Your updated information is accurate for all inputs/outputs as viewed at the last update before the time of your request.

ATTENTION: Do not set your real-time sample interval less than the slowest channel's update time.



Input Filtering

The input modules have selectable input filtering that is built into the A/D converter. The filter attenuates the input signal beginning at the specified frequency. You can select from 150, 300, 600, and 1200 Hz with low pass filters of none, 100 ms, 500 ms, or 1000 ms. Each channel filter can be set individually. Select the filter based on your system requirements.

A/D Conversion Rate	Low Pass Filter
1200 Hz	No low pass
1200 Hz	100 ms low pass
1200 Hz	500 ms low pass
1200 Hz	1000 ms low pass
600 Hz	No low pass
600 Hz	100 ms low pass
600 Hz	500 ms low pass
600 Hz	1000 ms low pass
300 Hz	No low pass
300 Hz	100 ms low pass
300 Hz	500 ms low pass
300 Hz	1000 ms low pass
150 Hz	No low pass
150 Hz	100 ms low pass
150 Hz	500 ms low pass
150 Hz	1000 ms low pass

Read Data from Your Module

Read programming moves status and data from the module to the processor's data table. The processor's user program initiates the request to transfer data from the input module (or combination module) to the processor.

Map Data for the Analog Modules

The following read and write words and bit/word descriptions describe the information that is written to and read from the analog modules. Each word is composed of 16 bits.

8 Input Analog Module — 1794-IF4I

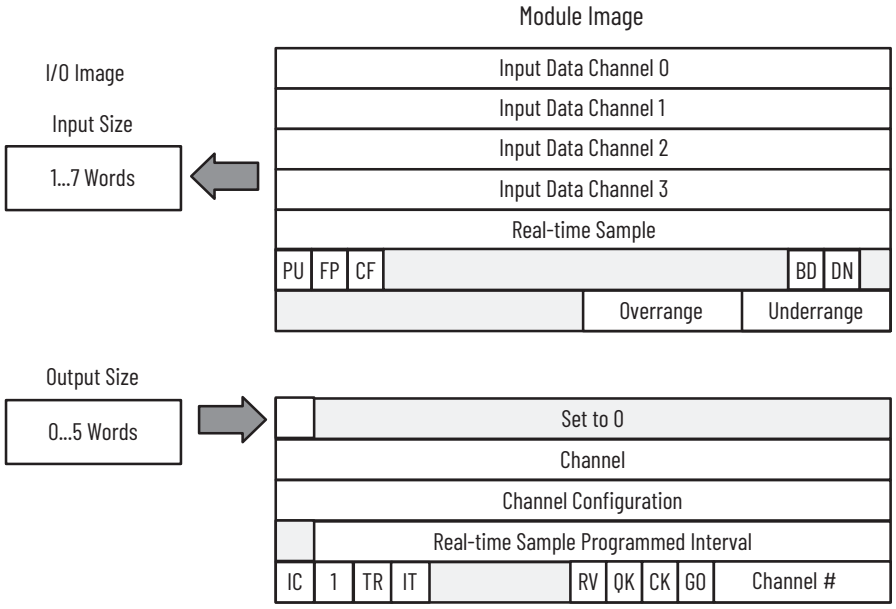


Table 3 - Analog Input Module — 1794-IF4I Read

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 0	Analog Value Channel 0															
Word 1	Analog Value Channel 1															
Word 2	Analog Value Channel 2															
Word 3	Analog Value Channel 3															
Word 4	Read-time Sample															
Word 5	PU	FP	CF	0		Reserved			0	0	0	0	0	BD	DN	0
Word 6	0	0	0	0	0	0	0	0	V3	V2	V1	V0	U3	U2	U1	U0

Where:
PU = Power-up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
U = Under range for specified channel
V = Overrange for specified channel

Table 4 - Word/Bit Descriptions for the 1794-IF4I Analog Input Module Read

Read Word	**Decimal Bit (Octal Bit)**	**Definition**
Word 0	Bits 00...15 (00...17)	**Channel 0 analog data** – Real-time input data per your configuration
Word 1	Bits 00...15 (00...17)	**Channel 1 analog data** – Real-time input data per your configuration
Word 2	Bits 00...15 (00...17)	**Channel 2 analog data** – Real-time input data per your configuration
Word 3	Bits 00...15 (00...17)	**Channel 3 analog data** – Real-time input data per your configuration
Word 4	Bits 00...15 (00...17)	**Real-time Sample** – The elapsed time in increments programmed by the real-time sample interval
Word 5	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN)** – This bit is set to 1 after a calibration cycle is completed.
	Bits 02	**Calibration Bad bit (BD)** – This bit is set to 1 if the channel calibration coefficients cannot be saved or read properly.
	Bits 03...07	Set to 0
	Bits 08...11 (10...12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the calibration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.

Table 4 - Word/Bit Descriptions for the 1794-IF4I Analog Input Module Read (Continued)

Read Word	Decimal Bit (Octal Bit)	Definition
Word 5	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU)** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 6	Bits 00...03	**Underrange bits (U)** – These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, and so on. See Table 8 on page 34.
	Bits 04...07	**Overrange bits (V)** – These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1, and so on. See Table 8 on page 34.
	Bits 08...15 (10...17)	Not used. Set to 0.

Table 5 - Analog Input Module — 1794-IF4I Write Configuration Block

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 0	EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Channel 3 Filter				Channel 2 Filter				Channel 1 Filter				Channel 0 Filter			
Word 2	Channel 3 Configuration				Channel 2 Configuration				Channel 1 Configuration				Channel 0 Configuration			
Word 3	0	Real-time Sample Programmed Interval														
Word 4	IC	1	TR	IT	0	0	0	0	RV	QK	CK	CO	Channel Number			

Where:
EN = Not used on the 1794-IF4I
IC = Initiate configuration bit
TR = Transparent bit
IT = Interrupt Toggle bit
RV = Revert to defaults bit
QK = Quick calibration
CK = Calibration clock
GO = Gain offset select

Table 6 - Word/Bit Descriptions for the 1794-IF4I Analog Input Module Write

Write Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00...14 (00...16)	Not used. Set to 0.
	Bits 15 (17)	**Output enable bit (EN)** – Not used in the 1794-IF4I module.
Word 1	Channels 0...3 Filter Selections (see Table 7 on page 34)	
	Bits 00...03	Channel 0 Filter Setting
	Bits 04...07	Channel 1 Filter Setting
	Bits 08...11 (10...13)	Channel 2 Filter Setting
	Bits 12...15 (14...17)	Channel 3 Filter Setting
Word 2	Channel Configuration (see Table 8 on page 34)	
	Bits 00...03	Channel 0 Configuration
	Bits 04...07	Channel 1 Configuration
	Bits 08...11 (10...13)	Channel 2 Configuration
	Bits 12...15 (14...17)	Channel 3 Configuration
Word 3	Bits 00...14 (00...16)	**Real-time Sample Interval** – Programs the interval of the real-time sample. Can be varied from 0...30 seconds (30,000 decimal). Resolution is in ms with granularity in 5 ms steps.
	Bit 15 (17)	Not used. Set to 0.
Word 4	Bits 00...03	**Channel calibration selection bit** – When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, bit 02 corresponds to input channel 2, bit 03 corresponds to input channel 3.
	Bit 04	**Gain/Offset selection bit (GO)** – When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK)** – When this bit is set to 1 (calibration mode), the calibration coefficient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for successful calibration.
	Bit 06	**Quick Calibration bit (QK)** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **Note:** This method of calibration quickly calibrates the selected channels, however you are not within the rated accuracy of the module.

Table 6 - Word/Bit Descriptions for the 1794-IF4I Analog Input Module Write (Continued)

Write Word	Decimal Bit (Octal Bit)	Definition
Word 4	Bit 07	**Revert to defaults bit (RV)** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **Note:** You are not within the rated accuracy of the module.
	Bits 08...11 (10...13)	Not used. Set to 0. **For IF4ICFXT only:** Bit 8 – **FastStepResponse (FR)** forces the A/D to skip the FIR stage if an input step occurs. An averaging algorithm is temporarily used instead of the FIR filter in the A/D to provide a quicker response. Bit 9 – **FIRFilterDisable (SK)** bypasses the FIR filter stage in the A/D. Bit 10 – **ChopModeDisable (CH)** disables the chop mode in the A/D. Chop mode is used to reduce offsets between input and output of the analog section of the A/D.(1) **Note:** Module level settings that only affect 150 Hz, 300 Hz, and 600 Hz conversion rate settings.
	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5 ms update rate are reduced to 5.0 ms. When reset (0), real-time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR)** – This bit, when set to 1, permits configuration to be changed without using the IC bit. Default setting for this bit is True (1).
	Bit 14 (16)	Always set to 1
	Bit 15 (17)	**Initiate Configuration bit (IC)** – When set (1), instructs the module to enter configuration mode. Present configuration data before or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subsequent configuration information is ignored until IC is toggled.

(1) For changes in tag values like the CH bit in the IF4ICFXT to take effect, the tag either must be included in a ladder rung or a configuration download that is forced using the configuration tab in the Studio 5000 Logix Designer application GUI.

Table 7 - Set Input Filter

Bits				Channel	
03	02	01	00	Input 0	
07	06	05	04	Input 1	
11	10	09	08	Input 2	
15	014	13	12	Input 3	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200 Hz	No low pass
0	0	0	1	1200 Hz	100 ms low pass
0	0	1	0	1200 Hz	500 ms low pass
0	0	1	1	1200 Hz	1000 ms low pass
0	1	0	0	600 Hz	No low pass
0	1	0	1	600 Hz	100 ms low pass
0	1	1	0	600 Hz	500 ms low pass
0	1	1	1	600 Hz	1000 ms low pass
1	0	0	0	300 Hz	No low pass
1	0	0	1	300 Hz	100 ms low pass
1	0	1	0	300 Hz	500 ms low pass
1	0	1	1	300 Hz	1000 ms low pass
1	1	0	0	150 Hz	No low pass
1	1	0	1	150 Hz	100 ms low pass
1	1	1	0	150 Hz	500 ms low pass
1	1	1	1	150 Hz	1000 ms low pass

Table 8 - Configure Your Input Module

Input Channel Configuration				
03	02	01	00	Set these bits for Channel 0
07	06	05	04	Set these bits for Channel 1
11	10	09	08	Set these bits for Channel 2
15	14	13	12	Set these bits for Channel 3

Table 8 - Configure Your Input Module (Continued)

Input Channel Configuration										
Bit Settings				Input Values	Data Format	% Underrange % Overrange	Input Range[1]		Module Update Rate	
							Hexadecimal	Decimal	(RTSI = 0)	(RTSI = 0) IT = 1
0	0	0	0	Channel not configured						
0	0	0	1	4...20 mA	Signed 2's complement	4% Under; 4% Over	<0000...7878>	<0000...30840>	7.5 ms	5.0 ms
0	0	1	0	±10V	Signed 2's complement	2% Under; 2% Over	<831F...7CE1>	<-31969...31969>	2.5 ms	2.5 ms
0	0	1	1	±5V	Signed 2's complement	4% Under; 4% Over	<8618...79E8>	<-31208...31208>	2.5 ms	2.5 ms
0	1	0	0	0...20 mA	Signed 2's complement %	0% Under; 4% Over	<0...2710>	<0...10000>	7.5 ms	5.0 ms
0	1	0	1	4...20 mA	Signed 2's complement %	4% Under; 4% Over	<0...2710>	<0...10000>	7.5 ms	5.0 ms
0	1	1	0	0...10V	Signed 2's complement %	0% Under; 2% Over	<0...2710>	<0...10000>	5.0 ms	5.0 ms
0	1	1	1	±10V	Signed 2's complement %	2% Under; 2% Over	<D8F0...2710>	<-10000...10000>	5.0 ms	5.0 ms
1	0	0	0	0...20 mA	Binary	0% Under; 4% Over	<0000...F3CF>	<0000...62415>	2.5 ms	2.5 ms
1	0	0	1	4...20 mA[2]	Binary	4% Under; 4% Over	<0000...F0F1>	<0000...61684>	7.5 ms	5.0 ms
1	0	1	0	0...10V	Binary	0% Under; 2% Over	<0000...F9C2>	<0000...63938>	2.5 ms	2.5 ms
1	0	1	1	0...5V	Binary	0% Under; 4% Over	<0000...F3CF>	<0000...62415>	2.5 ms	2.5 ms
1	1	0	0	0...20 mA	Offset binary, 8000 H = 0 mA	4% Under; 4% Over	<0618...F9E8>	<1560...63976>	2.5 ms	2.5 ms
1	1	0	1	4...20 mA	Offset binary, 8000 H = 4 mA	4% Under; 4% Over	<8000...F878>	<32768...63608>	7.5 ms	5.0 ms
1	1	1	0	±10V	Offset binary, 8000 H = 0V	2% Under; 2% Over	<031F...FCE1>	<799...64737>	2.5 ms	2.5 ms
1	1	1	1	±5V	Offset binary, 8000 H = 0V	4% Under; 4% Over	<0618...F9E8>	<1560...63976>	2.5 ms	2.5 ms

(1) < and > indicate the overrun beyond the actual range (about 5%).
(2) Underrange for 4...20 mA occurs in the blind area below 0 (3.2 mA).

4 Isolated Output Analog Module — 1794-OF4I

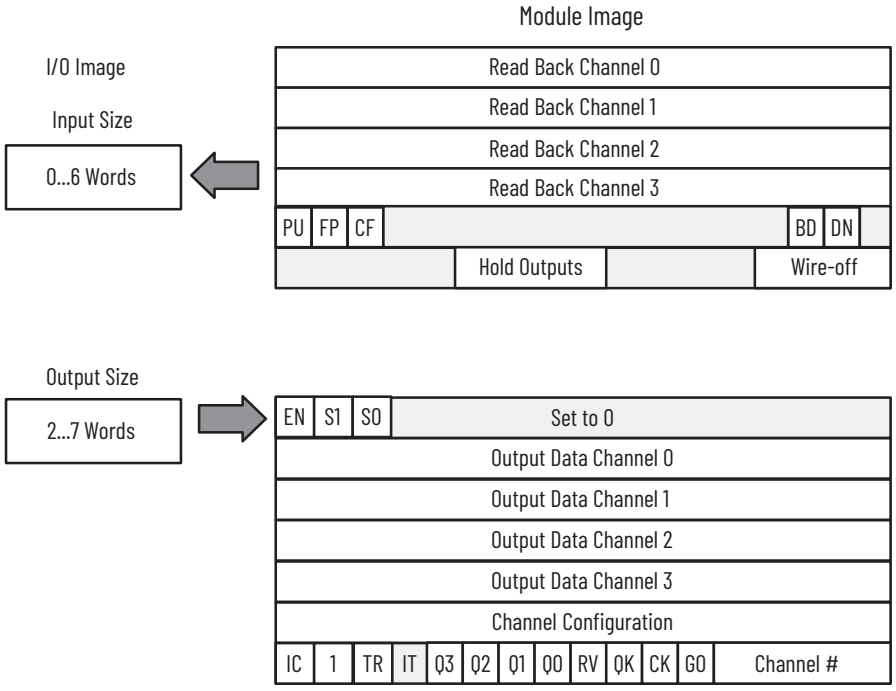


Table 9 - Analog Output Module — 1794-OF4I Read

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 0	Analog Value Channel 0															
Word 1	Analog Value Channel 1															
Word 2	Analog Value Channel 2															
Word 3	Analog Value Channel 3															
Word 4	PU	FP	CF	0		Reserved			0	0	0	0	0	BD	DN	0
Word 5	0	0	0	0	P3	P2	P1	P0	0	0	0	0	W3	W2	W1	W0

Where:
PU = Power-up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
P0…P3 = Output holding in response to Q0…Q3
W0…W3 = Wire off current loop status for channels 0…3 respectively (not used on voltage outputs)

Table 10 - Word/Bit Descriptions for the 1794-OF4I Analog Output Module Read

Read Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00…15 (00…17)	**Read Back Channel 0** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 1	Bits 00…15 (00…17)	**Read Back Channel 1** – During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 2	Bits 00…15 (00…17)	**Read Back Channel 2** – During normal operation, it is a copy of the output of channel 2. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 3	Bits 00…15 (00…17)	**Read Back Channel 3** – During normal operation, it is a copy of the output of channel 3. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 4	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN)** – This bit is set to 1 after a calibration cycle is completed.
	Bits 02	**Calibration Bad bit (BD)** – This bit is set to 1 if the channel calibration coefficients cannot be saved or read properly.
	Bits 03…07	Set to 0
	Bits 08…11 (10…12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the configuration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set, the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU)** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set, the module status indicator flashes.
Word 5	Bits 00…03	**Wire-Off status bits. (W)** – These bits, when set (1), indicate that the corresponding current output channel is open. W0 corresponds to channel 0, W1 corresponds to channel 2, and so on.
	Bits 04…07	Set to 0
	Bits 10…11 (12…13)	**Hold output bits (P)** – These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12…15 (14…17)	Set to 0

Table 11 - Analog Output Module — 1794-OF4I Write Configuration Block

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Write Word 0	EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Output Data – Channel 0															
Word 2	Output Data – Channel 1															
Word 3	Output Data – Channel 2															

Table 11 - Analog Output Module — 1794-OF4I Write Configuration Block (Continued)

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 4	Output Data – Channel 3															
Word 5	Output Ch 3 Configuration				Output Ch 3 2 Configuration				Output Ch 3 1 Configuration				Output Ch 3 0 Configuration			
Word 6	IC	1	TR	IT	0	0	0	0	RV	QK	CK	CO	Channel Number			

Where:
EN = Enable outputs; 0 = output follows S1/S0, 1 = output enabled
IC = Initiate configuration bit
TR = Transparent bit
IT = Interrupt Toggle bit
Q0...Q3 = Request for outputs to hold
RV = Revert to defaults bit
QK = Quick calibration
CK = Calibration clock
GO = Gain offset select

Table 12 - Range Selection Bits/Real-time Output Update – 1794-OF4I Isolated Output Module

Configuration Bits				Nominal Range	Data Type	Output Values		Update Rate
MSD		LSD				Hexadecimal	Decimal	
0	0	0	1	4...20 mA	Signed 2's complement	<0000...7878>	<0000...30840>	5.0 ms
0	0	1	0	±10V	Signed 2's complement	<8618...79E8>	<-31208...31208>	2.5 ms
0	0	1	1	±5V	Signed 2's complement	<8618...79E8>	<-31208...31208>	2.5 ms
0	1	0	0	0...20 mA	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	0	1	4...20 mA	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	1	0	0...10V	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	1	1	±10V	Signed 2's complement %	<D8F0...2710>	<-10000...10000>	5.0 ms
1	0	0	0	0...20 mA	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	0	1	4...20 mA	Binary	<0000...F0F1>	<0000...61681>	5.0 ms
1	0	1	0	0...10V	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	1	1	0...5V	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	1	0	0	0...20 mA	Offset binary	<8000...F9E8>	<32768...63976>	2.5 ms
1	1	0	1	4...20 mA	Offset binary	<8000...F878>	<32768...63608>	5.0 ms
1	1	1	0	±10V	Offset binary	<0618...F9E8>	<1560...63976>	2.5 ms
1	1	1	1	±5V	Offset binary	<0618...F9E8>	<1560...63976>	2.5 ms

Table 13 - Word/Bit Descriptions for the 1794-OF4I Analog Output Module Write

Write Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00...12 (00...14)	Not used
	Bits 13...14 (15...16)	**Safe State Source bits (S1/S0)** – When EN is 0, these bits designate the source of the safe state data. Bit 13 = 0, bit 14 = 1 – reset outputs to 0V/0mA (used with 1794-ASB/C) Bit 13 = 1, bit 14 = 1 – hold output at its current level (used with 1794-ASB/C) Bit 13 = 0; bit 14 = 0 – Safe state data is in output data words
	Bits 15 (17)	**Output enable bit (EN)** – When set (1), the outputs are enabled. This bit must be set in order for the real-time data to appear at the outputs. If this bit is not set (0), then S1/S0 determines the outputs.
Word 1	Bits 00...15 (00...17)	**Channel 0 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 2	Bits 00...15 (00...17)	**Channel 1 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 3	Bits 00...15 (00...17)	**Channel 2 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 4	Bits 00...15 (00...17)	**Channel 3 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 5	**Channel Configuration**	
	Bits 00...03	Channel 0 Configuration
	Bits 04...07	Channel 1 Configuration
	Bits 08...11 (10...13)	Channel 2 Configuration
	Bits 12...15 (14...17)	Channel 3 Configuration

Table 13 - Word/Bit Descriptions for the 1794-OF4I Analog Output Module Write (Continued)

Write Word	Decimal Bit (Octal Bit)	Definition
Word 6	Bits 00...03	**Channel calibration selection bit** – When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to output channel 0, bit 01 corresponds to output channel 1, it 02 corresponds to output channel 3, bit 03 corresponds to output channel 4.
	Bit 04	**Gain/Offset selection bit (GO)** – When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK)** – When this bit is set to 1 (calibration mode), the calibration coefficient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for successful calibration.
	Bit 06	**Quick Calibration bit (QK)** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **Note:** Although this method of calibration quickly calibrates the selected channels, they are not within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV)** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **Note:** They are not within the rated accuracy of the module.
	Bits 08...11 (10...13)	**Request for hold outputs (Q)** – Channel request bits that instruct an output to hold its output level when EN transitions from 1 to 0 to 1. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs hold their level until the output data equals the output level. P0–P3 indicates channels holding. Output readback data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 09 (11) = channel 1, and so on.
	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5 ms update rate are reduced to 5.0 ms. When reset (0), real-time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR)** – This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 14 (16)	Set to 1
	Bit 15 (17)	**Initiate Configuration bit (IC)** – When set (1), instructs the module to enter configuration mode. Present configuration data before or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subsequent configuration information is ignored until IC is toggled.

2 Input/2 Output Analog Combo Module — 1794-IF2XOF2I

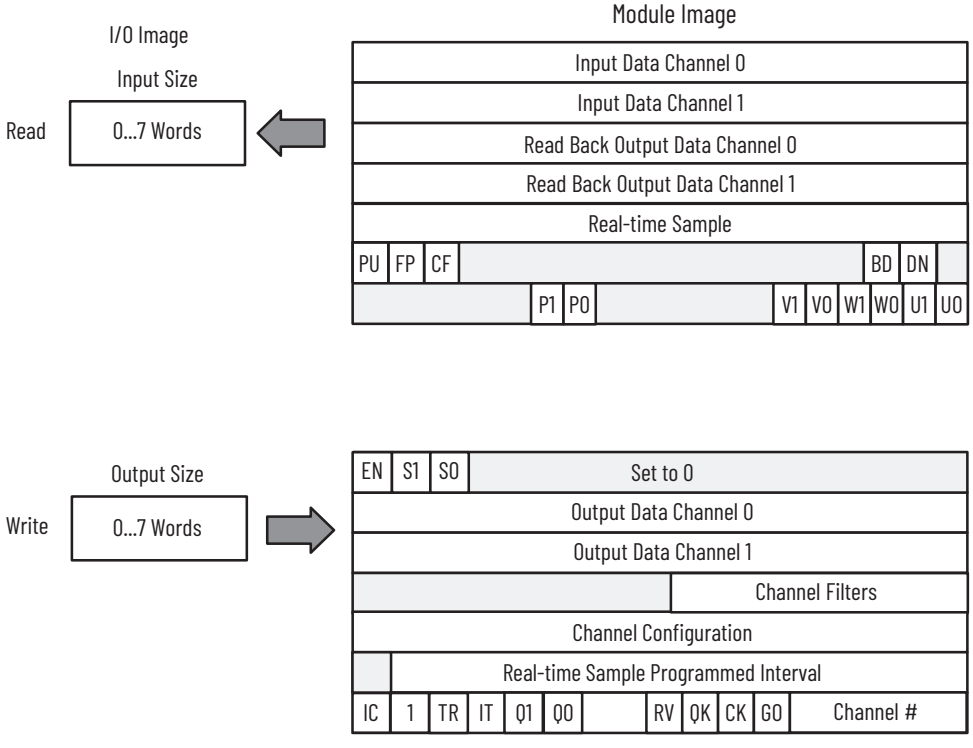


Table 14 - Analog Combo Module — 1794-IF2XOF2I Read

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 0	Input Data Channel 0															
Word 1	Input Data Channel 1															
Word 2	Read Back Output Channel 0															
Word 3	Read Back Output Channel 1															
Word 4	0	Real-time Sample														
Word 5	PU	FP	CF	0	Reserved				0	0	0	0	0	BD	DN	0
Word 6	0	0	0	0	P1	P0	0	0	0	0	V1	V0	W1	W0	U1	U0

Where:
PU = Power-up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
P0 and P1 = Output holding in response to Q0...Q1
W0 and W1 = Wire off current loop status for input channels 0 and 1 respectively (not used on voltage outputs)
U0 and U1 = Underrange for input channels 0 and 1 respectively
V0 and V1 = Overrange for input channels 0 and 1 respectively

Table 15 - Configure Your Input Channels

Input Channel Configuration									
03	02	01	00	Set these bits for Channel 0					
07	06	05	04	Set these bits for Channel 1					
Bit Settings				**Input Values**	**Data Format**	**% Underrange % Overrange**	**Input Range[1]**		**Module Update Rate**	
							Hexadecimal	**Decimal**	**(RTSI = 0)**	**(RTSI = 0) IT = 1**
0	0	0	0	Channel not configured						
0	0	0	1	4...20 mA	Signed 2's complement	4% Under; 4% Over	<0000...7878>	<0000...30840>	7.5 ms	5.0 ms
0	0	1	0	±10V	Signed 2's complement	2% Under; 2% Over	<831F...7CE1>	<-31969...31969>	2.5 ms	2.5 ms
0	0	1	1	±5V	Signed 2's complement	4% Under; 4% Over	<8618...79E8>	<-31208...31208>	2.5 ms	2.5 ms
0	1	0	0	0...20 mA	Signed 2's complement %	0% Under; 4% Over	<0...2710>	<0...10000>	7.5 ms	5.0 ms
0	1	0	1	4...20 mA	Signed 2's complement %	4% Under; 4% Over	<0...2710>	<0...10000>	7.5 ms	5.0 ms
0	1	1	0	0...10V	Signed 2's complement %	0% Under; 2% Over	<0...2710>	<0...10000>	5.0 ms	5.0 ms
0	1	1	1	±10V	Signed 2's complement %	2% Under; 2% Over	<D8F0...2710>	<-10000...10000>	5.0 ms	5.0 ms
1	0	0	0	0...20 mA	Binary	0% Under; 4% Over	<0000...F3CF>	<0000...62415>	2.5 ms	2.5 ms
1	0	0	1	4...20 mA[2]	Binary	4% Under; 4% Over	<0000...F0F1>	<0000...61681>	7.5 ms	5.0 ms
1	0	1	0	0...10V	Binary	0% Under; 2% Over	<0000...F9C2>	<0000...63938>	2.5 ms	2.5 ms
1	0	1	1	0...5V	Binary	0% Under; 4% Over	<0000...F3CF>	<0000...62415>	2.5 ms	2.5 ms
1	1	0	0	0...20 mA	Offset binary, 8000 H = 0 mA	4% Under; 4% Over	<0618...F9E8>	<1560...63976>	2.5 ms	2.5 ms
1	1	0	1	4...20 mA	Offset binary, 8000 H = 4 A	4% Under; 4% Over	<8000...F878>	<32768...63608>	7.5 ms	5.0 ms
1	1	1	0	±10V	Offset binary, 8000 H = 0 mA	2% Under; 2% Over	<031F...FCE1>	<799...64737>	2.5 ms	2.5 ms
1	1	1	1	±5V	Offset binary, 8000 H = 0 mA	4% Under; 4% Over	<0618...F9E8>	<1560...63976>	2.5 ms	2.5 ms

(1) < and > indicate the overrun beyond the actual range (about 5%).
(2) Underrange for 4...20 mA occurs in the blind area below 0 (3.2 mA).

Table 16 - Set Input Filter

Bits				Channel	
03	02	01	00	Input Channel 0	
07	06	05	04	Input Channel 1	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200 Hz	No low pass
0	0	0	1	1200 Hz	100 ms low pass
0	0	1	0	1200 Hz	500 ms low pass

Table 16 - Set Input Filter (Continued)

Bits				Channel	
0	0	1	1	1200 Hz	1000 ms low pass
0	1	0	0	600 Hz	No low pass
0	1	0	1	600 Hz	100 ms low pass
0	1	1	0	600 Hz	500 ms low pass
0	1	1	1	600 Hz	1000 ms low pass
1	0	0	0	300 Hz	No low pass
1	0	0	1	300 Hz	100 ms low pass
1	0	1	0	300 Hz	500 ms low pass
1	0	1	1	300 Hz	1000 ms low pass
1	1	0	0	150 Hz	No low pass
1	1	0	1	150 Hz	100 ms low pass
1	1	1	0	150 Hz	500 ms low pass
1	1	1	1	150 Hz	1000 ms low pass

Table 17 - Word/Bit Descriptions for the 1794-IF2X0F2I Isolated Analog Combo Module Read

Read Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00...15 (00...17)	**Input Channel 0 input data** – Real-time input data per your configuration
Word 1	Bits 00...15 (00...17)	**Input Channel 1 input data** – Real-time input data per your configuration
Word 2	Bits 00...15 (00...17)	**Read Back Output Channel 0** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. **Note:** Readback data is an image of what you have sent as output to the module; no checks are performed on the data.
Word 3	Bits 00...15 (00...17)	**Read Back Output Channel 1** – During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0. **Note:** Readback data is an image of what you have sent as output to the module; no checks are performed on the data.
Word 4	Bits 00...15 (00...17)	**Real-time Sample** – The elapsed time in increments programmed by the real-time sample interval
Word 5	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN)** – This bit is set to 1 after a calibration cycle is completed.
	Bits 02	**Calibration Bad bit (BD)** – This bit is set to 1 if the channel calibration coefficients cannot be saved or read properly.
	Bits 03...07	Set to 0
	Bits 08...11 (10...12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the configuration mode is selected (bit 15, word 6 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU)** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 6	Bits 00...01	**Underrange bits (U)** – These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, and so on. See Table 15 on page 39.
	Bits 02...03	**Wire-Off status bits. (W)** – These bits, when set (1), indicate that the corresponding current output channel is open. W0 corresponds to channel 0, W1 corresponds to channel 2, and so on.
	Bits 04...05	**Overrange bits (V)** – These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1. See Table 15 on page 39.
	Bits 06...09 (06...11)	Not used. Set to 0.
	Bits 10...11 (12...13)	**Hold output bits (P)** – These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12...15 (14...17)	Not used. Set to 0.

Table 18 - Analog Combo Module — 1794-IF2X0F2I Read

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Write Word 0	EN	S1	S0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Output Data – Channel 0															
Word 2	Output Data – Channel 1															
Word 3	0	0	0	0	0	0	0	0	Input Ch 1 Filter				Input Ch 0 Filter			
Word 4	Output Ch 1 Configuration				Output Ch 0 2 Configuration				Output Ch 1 Configuration				Output Ch 0 Configuration			
Word 5	0	Real-time Sample Programmed Interval														
Word 6	IC	1	TR	IT	Q1	Q2	0	0	RV	QK	CK	G0	Input Ch 0 Configuration			

Where:
EN = Enable outputs; 0 = Output follows S1/S0, 1 = Output enabled
IC = Initiate configuration bit
IT = Interrupt Toggle bit
TR = Transparent bit
Q0 and Q1 = Request for outputs to hold
RV = Revert to defaults bit
QK = Quick calibration
CK = Calibration clock
G0 = Gain offset select

Table 19 - Configure Your Outputs for the 1794-IF2X0F2I Analog Combo Module

Configuration Bits				Nominal Range	Data Type	Output Values[1]		Update Rate
MSD		LSD				Hexadecimal	Decimal	
0	0	0	1	4...20 mA	Signed 2's complement	<0000-7878>	<0000-30840>	5.0 ms
0	0	1	0	±10V	Signed 2's complement	<8618-79E8>	<-31208-31208>	2.5 ms
0	0	1	1	±5V	Signed 2's complement	<8618-79E8>	<-31208-31208>	2.5 ms
0	1	0	0	0...20 mA	Signed 2's complement %	<0-2710>	<0-10000>	5.0 ms
0	1	0	1	4...20 mA	Signed 2's complement %	<0-2710>	<0-10000>	5.0 ms
0	1	1	0	0...10V	Signed 2's complement %	<0-10000>	<0-10000>	5.0 ms
0	1	1	1	±10V	Signed 2's complement %	<D8F0-2710>	<-10000-10000>	5.0 ms
1	0	0	0	0...20 mA	Binary	<0000-F3CF>	<0000-62415>	2.5 ms
1	0	0	1	4...20 mA	Binary	<0000-F0F1>	<0000-61681>	5.0 ms
1	0	1	0	0...10V	Binary	<0000-F3CF>	<0000-62415>	2.5 ms
1	0	1	1	0...5V	Binary	<0000-F3CF>	<0000-62415>	2.5 ms
1	1	0	0	0...20 mA	Offset binary	<8000-F9E8>	<32768-63976>	2.5 ms
1	1	0	1	4...20 mA	Offset binary	<8000-F878>	<32768-63608>	5.0 ms
1	1	1	0	±10V	Offset binary	<0618-F9E8>	<1560-63976>	2.5 ms
1	1	1	1	±5V	Offset binary	<0618-F9E8>	<1560-63976>	2.5 ms

(1) < and > indicate the overrun beyond the actual range (about 5%).

Table 20 - Word/Bit Descriptions for the 1794-IF2X0F2I Analog Combo Module Write

Write Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00...14 (00...16)	Not used
	Bits 13...14 (15...16)	**Safe State Source bits (S1/S0)** – When EN is 0, these bits designate the source of the safe state data. Bit 13 = 0, bit 14 = 1 – reset outputs to 0V/0mA (used with 1794-ASB/C) Bit 13 = 1, bit 14 = 1 – hold output at its current level (used with 1794-ASB/C) Bit 13 = 0; bit 14 = 0 – Safe state data is in output data words
	Bits 15 (17)	**Output enable bit (EN)** – When set (1), the outputs are enabled. This bit must be set in order for the real-time data to appear at the outputs. If this bit is not set (0), then S1/S0 determines the outputs.
Word 1	Bits 00...15 (00...17)	**Channel 0 output data** – See Table 19 on page 41
Word 2	Bits 00...15 (00...17)	**Channel 1 output data** – See Table 19 on page 41
Word 3	**Input Channels 0 and 1 Filter Selections** – See Table 16 on page 39	
	Bits 00...01	Channel 0 Filter Setting
	Bits 04...07	Channel 1 Filter Setting

Table 20 - Word/Bit Descriptions for the 1794-IF2XOF2I Analog Combo Module Write (Continued)

Write Word	Decimal Bit (Octal Bit)	Definition
Word 4	**Channel Configuration** – See Table 15 on page 39	
	Bits 00…03	**Input Channel 0 Configuration** – See Table 15 on page 39
	Bits 04…07	**Input Channel 1 Configuration** – See Table 15 on page 39
	Bits 08…11 (10…13)	**Output Channel 0 Configuration** – See Table 19 on page 41
	Bits 12…15 (14…17)	**Output Channel 1 Configuration** – See Table 19 on page 41
Word 5	Bits 00…14 (00…16)	**Real-time Sample Interval** – Programs the interval of the real-time sample. Can be varied 0….30 seconds (30,000 decimal). Resolution is in ms with granularity in 5 ms steps. See Table 2 on page 30.
Word 6	Bits 00…03	**Channel calibration selection bit** – When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to output channel 0, bit 01 corresponds to output channel 1, it 02 corresponds to output channel 3, bit 03 corresponds to output channel 4.
	Bit 04	**Gain/Offset selection bit (GO)** – When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK)** – When this bit is set to 1 (calibration mode), the calibration coefficient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for successful calibration.
	Bit 06	**Quick Calibration bit (QK)** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **Note:** Although this method of calibration quickly calibrates the selected channels, they are not within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV)** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **Note:** They are not within the rated accuracy of the module.
	Bits 08…09 (10…11)	Not used. Set to 0.
	Bit 10…11 (12…13)	**Request for hold outputs (Q)** – Channel request bits that instruct an output to hold its output level when EN transitions from 1 to 0 to 1. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs hold their level until the output data equals the output level. P0–P3 indicates channels holding. Output readback data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 08 (10) = channel 1, and so on.
	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5 ms update rate are reduced to 5.0 ms. When reset (0), real-time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR)** – This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 15 (17)	**Initiate Configuration bit (IC)** – When set (1), instructs the module to enter configuration mode. Present configuration data before or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subsequent configuration information is ignored until IC is toggled.

Communication and I/O Image Table Mapping with the DeviceNet/ControlNet Adapter

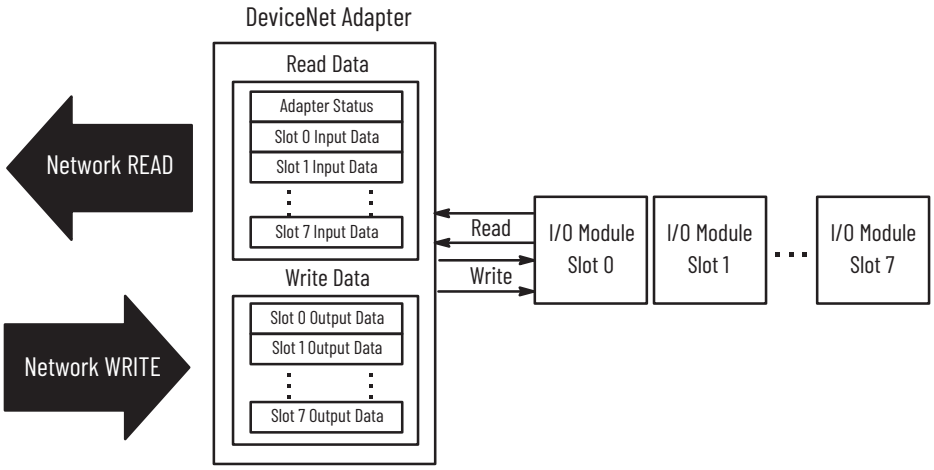
About RSNetWorx and Studio 5000 Logix Designer

RSNetWorx™ is a software tool that is used with Studio 5000 Logix Designer application to configure your FLEX I/O DeviceNet or ControlNet adapter and its related modules. This software tool can be connected to the adapter via the DeviceNet network. The EtherNet/IP adapter only requires Studio 5000 Logix Designer application to configure the modules.

Polled I/O Structure

The adapter receives the output data in the order of the installed I/O modules. The output data for slot 0 is received first, followed by the output data for slot 1, and so on, to slot 7.

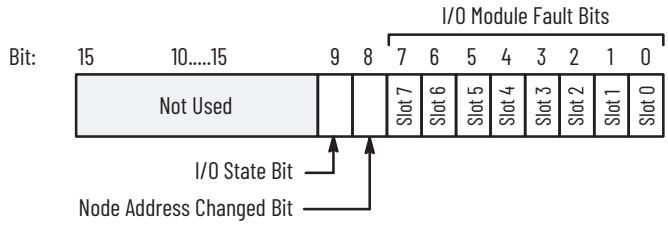
The first word of input data that the adapter sends is the Adapter Status Word. This is followed by the input data from each slot, in the order of installed I/O modules. The input data from slot 0 is first after the status word, followed by input data from slot 2, and so on, to slot 7.



Adapter Input Status Word

The input status word consists of:

- I/O module fault bits – 1 status bit for each slot
- Node address changed – 1 bit
- I/O status – 1 bit



The adapter input status word bit descriptions are shown in the following table.

Bit Description	Bit	Explanation
I/O Module Faults	0	This bit is set (1) when an error is detected in slot position 0.
	1	This bit is set (1) when an error is detected in slot position 1.
	2	This bit is set (1) when an error is detected in slot position 2.
	3	This bit is set (1) when an error is detected in slot position 3.
	4	This bit is set (1) when an error is detected in slot position 4.
	5	This bit is set (1) when an error is detected in slot position 5.
	6	This bit is set (1) when an error is detected in slot position 6.
	7	This bit is set (1) when an error is detected in slot position 7.
Node Address Changed	8	This bit is set (1) when the node address switch setting has been changed since power-up.
I/O Status	9	Bit = 0 – idle Bit = 1 – run
—	10...15	Not used – sent as zeros

Possible causes for an **I/O Module Fault** are:

- Transmission errors on the FLEX I/O backplane
- A failed module
- A module removed from its terminal base
- Incorrect module insertion in a slot position
- The slot is empty

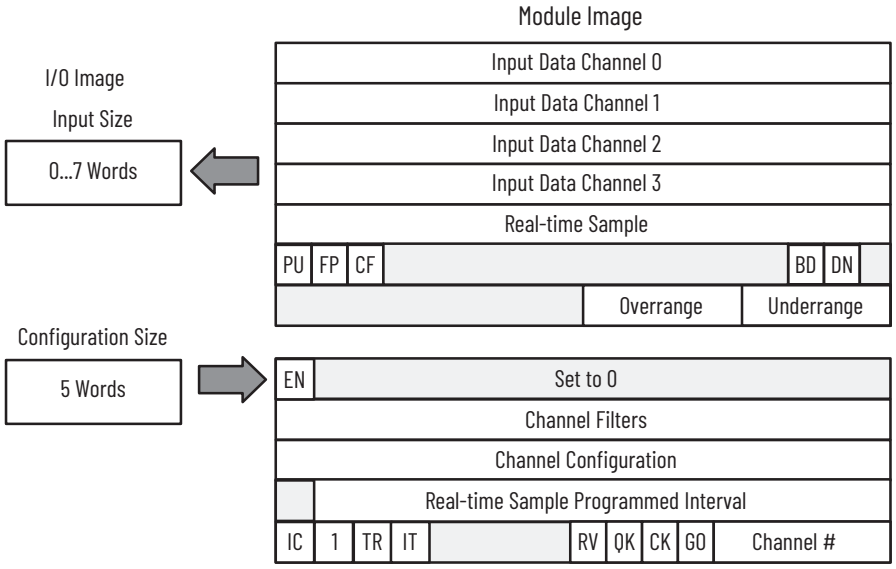
The **node address changed** bit is set when the node address switch setting has been changed since power-up. The new node address does not take effect until the adapter has been powered down and then powered backup.

Map Data into the Image Table

FLEX I/O analog modules are supported by the DeviceNet adapter.

Module Description	Catalog Number	For image table mapping, see:
4 Input Isolated Analog Module	1794-IF4I	4 Input Isolated Analog Module — 1794-IF4I Image Table Mapping
4 Output Isolated Analog Module	1794-OF4I	4 Output Isolated Analog Module — 1794-OF4I Image Table Mapping
2 in/2 out Isolated Analog Combo Module	1794-IF2XOF2I	Isolated Analog Combo Module — 1794-IF2XOF2I Series B Image Table Mapping

4 Input Isolated Analog Module — 1794-IF4I Image Table Mapping



Set EN bit to Off (0) for the Configuration block.
Module actions (Reset, Safe State, and Hold Last State) are set using programming software.

Table 21 - Analog Input Module — 1794-IF4I and 1794-IF4ICFXT Read

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 0	Analog Value Channel 0															
Word 1	Analog Value Channel 1															
Word 2	Analog Value Channel 2															
Word 3	Analog Value Channel 3															
Word 4	Real-time Sample															
Word 5	PU	FP	CF	0		Reserved			0	0	0	0	0	BD	DN	0
Word 6	0	0	0	0	0	0	0	0	V3	V2	V1	V0	U3	U2	U1	U0

Where:
PU = Power-up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
U = Under range for specified channel
V = Overrange for specified channel

Table 22 - Analog Input Module — 1794-IF4ICFXT Write

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 0	EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Ch 3 Filter				Ch 2 Filter				Ch 1 Filter				Ch 0 Filter			
Word 2	Ch 3 Configuration				Ch 2 Configuration				Ch 1 Configuration				Ch 0 Configuration			
Word 3	0	Real-time Sample Interval														

Table 22 - Analog Input Module — 1794-IF4ICFXT Write (Continued)

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 4	IC	1	TR	IT	0	CH	DK	FS	RV	QK	CK	GO	Channel Number			
Word 5	Reserved															

Where:
EN = Enable bit (not used on input module)
IC = Initiate Configuration bit
TR = Transparent bit
IT = Interrupt toggle bit
CH = Chop Mode Disable — use to disable the chop mode. Chop mode used by the module to reduce offset and drift errors. The default is chop mode enabled (0).
DK = FIR Filter Disable — use to disable the FIR filter. The Finite Impulse Response filter is used by the module to improve signal stability. The default is FIR filter enabled (0).
FS = Fast Step Response — use to enable a fast step response algorithm. The fast step response algorithm, upon sensing a step input, uses an averaging method rather than the FIR filter. The FIR returns to operation once the input has settled. The default is fast step response disabled (0).
RV = Revert to default bit
QK = Quick calibration
CK = Calibration clock
GO = Gain Offset select

Table 23 - Analog Input Module — 1794-IF4I Write Configuration Block

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 0	EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Ch 3 Filter				Ch 2 Filter				Ch 1 Filter				Ch 0 Filter			
Word 2	Ch 3 Configuration				Ch 2 Configuration				Ch 1 Configuration				Ch 0 Configuration			
Word 3	0	Real-time Sample Interval														
Word 4	IC	1	TR	IT	0	CH	DK	FS	RV	QK	CK	GO	Channel Number			
Word 5	Reserved															
Word 6	Not used															
Word 7	Not used															

Where:
EN = Not used on the 1794-IF4I
IC = Initiate configuration bit
TR = Transparent bit
IT = Interrupt Toggle bit
RV = Revert to defaults bit
QK = Quick calibration
CK = Calibration clock
GO = Gain offset select

Table 24 - Set Input Filter

Bits				Channel	
03	02	01	00	Input 0	
07	06	05	04	Input 1	
11	10	09	08	Input 2	
15	014	13	12	Input 3	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200 Hz	No low pass
0	0	0	1	1200 Hz	100 ms low pass
0	0	1	0	1200 Hz	500 ms low pass
0	0	1	1	1200 Hz	1000 ms low pass
0	1	0	0	600 Hz	No low pass
0	1	0	1	600 Hz	100 ms low pass
0	1	1	0	600 Hz	500 ms low pass
0	1	1	1	600 Hz	1000 ms low pass
1	0	0	0	300 Hz	No low pass
1	0	0	1	300 Hz	100 ms low pass
1	0	1	0	300 Hz	500 ms low pass
1	0	1	1	300 Hz	1000 ms low pass
1	1	0	0	150 Hz	No low pass
1	1	0	1	150 Hz	100 ms low pass
1	1	1	0	150 Hz	500 ms low pass
1	1	1	1	150 Hz	1000 ms low pass

Table 25 - Word/Bit Descriptions for 1794-IF4I Isolated Analog Input Module

Word	Decimal Bit (Octal Bit)	Definition
Read Word 0	Bits 00…15 (00…17)	**Channel 0 analog data** – Real-time input data per your configuration
Word 1	Bits 00…15 (00…17)	**Channel 1 analog data** – Real-time input data per your configuration
Word 2	Bits 00…15 (00…17)	**Channel 2 analog data** – Real-time input data per your configuration
Word 3	Bits 00…15 (00…17)	**Channel 3 analog data** – Real-time input data per your configuration
Word 4	Bits 00…15 (00…17)	**Real-time Sample** – The elapsed time in increments programmed by the real-time sample interval
Word 5	Bit 00	Reserved
	Bit 01	**Calibration Done bit (DN)** – This bit is set to 1 after a calibration cycle is completed.
	Bit 02	**Calibration Bad bit (BD)** – This bit is set to 1 if the channel calibration coefficients cannot be saved or be read properly.
	Bits 03…07	Set to 0
	Bits 08…11 (10…13)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the calibration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU)** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 6	Bits 00…03	**Underrange bits (U)** – These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, and so on.
	Bits 04…07	**Overrange bits (V)** – These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1, and so on.
	Bits 08…15 (10…17)	Not used. Set to 0.
Write Word 0	Bits 00…14 (00…16)	Not used. Set to 0.
	Bit 15 (17)	**Output enable bit (EN)** – Not used in the 1794-IF4I module
Word 1	Channels 0…3 Filter Selections	
	Bits 00…03	Channel 0 Filter Setting
	Bits 04…07	Channel 1 Filter Setting
	Bits 08…11 (00…13)	Channel 2 Filter Setting
	Bits 12…15 (14…17)	Channel 3 Filter Setting
Word 2	Channels 0…3 Filter Selections	
	Bits 00…03	Channel 0 Configuration
	Bits 04…07	Channel 1 Configuration
	Bits 08…11 (10…13)	Channel 2 Configuration
	Bits 12…15 (14…17)	Channel 3 Configuration
Word 3	Bits 00…14 (00…16)	**Real-time Sample Interval** – Programs the interval of the real-time sample. Can be varied from 0…30 seconds (30,000 decimal). Resolution is in ms with granularity in 5 ms steps.
	Bit 15 (17)	Not used. Set to 0.

Table 25 - Word/Bit Descriptions for 1794-IF4I Isolated Analog Input Module (Continued)

Word	Decimal Bit (Octal Bit)	Definition
Word 4	Bits 00...03	**Channel calibration selection bit** – When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, it 02 corresponds to input channel 2, bit 03 corresponds to input channel 3.
	Bit 04	**Gain/Offset selection bit (GO)** – When this bit is cleared, a 0...1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK)** – When this bit is set to 1 (calibration mode), the calibration coefficient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for successful calibration.
	Bit 06	**Quick Calibration bit (QK)** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **Note:** This method of calibration quickly calibrates the selected channels, however you are not within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV)** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **Note:** You are not within the rated accuracy of the module.
	Bits 08...11 (10...13)	Not used. Set to 0. **For IF4ICFXT only:** Bit 8 — **FastStepResponse (FR)** forces the A/D to skip the FIR stage if an input step occurs. An averaging algorithm is temporarily used instead of the FIR filter in the A/D to provide a quicker response. Bit 9 — **FIRFilterDisable (SK)** bypasses the FIR filter stage in the A/D. Bit 10 — **ChopModeDisable (CH)** disables the chop mode in the A/D. Chop mode is used to reduce offsets between input and output of the analog section of the A/D.(1) **Note:** Module level settings that only affect 150 Hz, 300 Hz, and 600 Hz conversion rate settings.
	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5 ms update rate are reduced to 5.0 ms. When reset (0), real-time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR)** – This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 15 (17)	**Initiate Configuration bit (IC)** – When set (1), instructs the module to enter configuration mode. Present configuration data before or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subsequent configuration information is ignored until IC is toggled.
Words 5	Bits 00...15 (00...17)	Not used

(1) For changes in tag values like the CH bit in the 1794-IF4ICFXT to take effect, the tag either must be included in a ladder rung or a configuration download that is forced using the configuration tab in the Studio 5000 Logix Designer application GUI.

4 Output Isolated Analog Module — 1794-OF4I Image Table Mapping

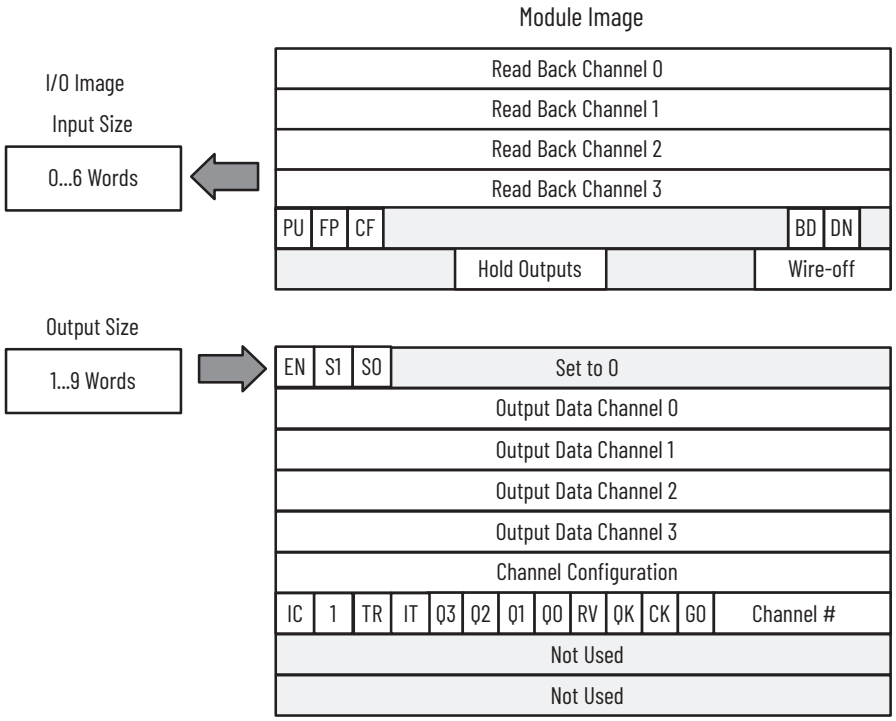


Table 26 - Analog Output Module — 1794-OF4I Read

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 0	Read Back Channel 0															
Word 1	Read Back Channel 1															
Word 2	Read Back Channel 2															
Word 3	Read Back Channel 3															
Word 4	PU	FP	CF	0	Reserved				0	0	0	0	0	BD	DN	0
Word 5	0	0	0	0	P3	P2	P1	P0	0	0	0	0	W3	W2	W1	W0

Where:
PU = Power-up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
P0...P3 = Output holding in response to Q0...Q3
W0...W3 = Wire off current loop status for channels 0...3 respectively. Not used on voltage outputs.

Table 27 - Analog Output Module — 1794-OF4I Write Configuration Block

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Write Word 0	EN	S1	S0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Output Data — Channel 0															
Word 2	Output Data — Channel 1															
Word 3	Output Data — Channel 2															
Word 4	Output Data — Channel 3															
Word 5	Output Ch 3 Configuration				Output Ch 2 Configuration				Output Ch 1 Configuration				Output Ch 0 Configuration			

Table 27 - Analog Output Module — 1794-OF4I Write Configuration Block (Continued)

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 6	IC	1	TR	IT	Q3	Q2	Q1	Q0	RV	QK	CK	GO	Channel Number			
Word 7	Not used															

Where:
EN = Enable outputs; 0 = Output follows S1/S0, 1 = Output enabled
IC = Initiate configuration bit
TR = Transparent bit
IT = Interrupt Toggle bit
Q0...Q3 = Request for outputs to hold
RV = Revert to defaults bit
QK = Quick calibration
CK = Calibration clock
GO = Gain offset select

Table 28 - Configure Outputs for 1794-OF4I Isolated Output Module

Configuration Bits				Nominal Range	Data Type	Output Values		Update Rate
MSD		LSD				Hexadecimal	Decimal	
0	0	0	1	4...20 mA	Signed 2's complement	<0000...7878>	<0000...30840>	5.0 ms
0	0	1	0	±10v	Signed 2's complement	<8618...79E8>	<-31208...31208>	2.5 ms
0	0	1	1	±5V	Signed 2's complement	<8618...79E8>	<-31208...31208>	2.5 ms
0	1	0	0	0...20 mA	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	0	1	4...20 mA	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	1	0	0...10V	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	1	1	±10V	Signed 2's complement %	<D8F0...2710>	<-10000...10000>	5.0 ms
1	0	0	0	0...20 mA	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	0	1	4...20 mA	Binary	<0000...F0F1>	<0000...61681>	5.0 ms
1	0	1	0	0...10V	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	1	1	0...5V	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	1	0	0	0...20 mA	Offset binary	<8000...F9E8>	<32768...63976>	2.5 ms
1	1	0	1	4...20 mA	Offset binary	<8000...F878>	<32768...63608>	5.0 ms
1	1	1	0	±10V	Offset binary	<0618...F9E8>	<1560...63976>	2.5 ms
1	1	1	1	±5V	Offset binary	<0618...F9E8>	<1560...63976>	2.5 ms

Table 29 - Word/Bit Descriptions for 1794-OF4I Isolated Analog Output Module

Word	Decimal Bit (Octal Bit)	Definition
Read Word 0	Bits 00...15 (00...17)	**Read Back Channel 0** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 1	Bits 00...15 (00...17)	**Read Back Channel 1** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 2	Bits 00...15 (00...17)	**Read Back Channel 2** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 3	Bits 00...15 (00...17)	**Read Back Channel 3** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 4	Bit 00	Reserved
	Bit 01	**Calibration Done bit (DN)** – This bit is set to 1 after a calibration cycle is completed.
	Bit 02	**Calibration Bad bit (BD)** – This bit is set to 1 if the channel calibration coefficients cannot be saved or be read properly.
	Bits 03...07	Set to 0
	Bits 08...11 (10...13)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the calibration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.

Table 29 - Word/Bit Descriptions for 1794-OF4I Isolated Analog Output Module (Continued)

Word	Decimal Bit (Octal Bit)	Definition
Word 4	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU)** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 5	Bits 00…03	**Wire-Off status bits. (W)** – These bits, when set (1), indicate that the corresponding current output channel is open. W0 corresponds to channel 0, W1 corresponds to channel 2, and so on.
	Bits 04…07	Set to 0
	Bits 10…11 (12…13)	**Hold output bits (P)** – These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12…15 (14…17)	Set to 0
Write Word 0	Bits 00…12 (00…14)	Not used
	Bit 13…14 (15…16)	**Safe State Source bits (S1/S0)** – When EN is 0, these bits designate the source of the safe state data. Bit 13 = 0, bit 14 = 1 – Reset outputs to 0V/0mA (used with 1794-ASB/C) Bit 13 = 1, bit 14 = 1 – Hold output at its current level (used with 1794-ASB/C) Bit 13 = 0; bit 14 = 0 – Safe state data is in output data words
	Bit 15 (17)	**Output enable bit (EN)** – When set (1), the outputs are enabled. This bit must be set in order for the real-time data to appear at the outputs. If this bit is not set (0), then S1/S0 determines the outputs.
Word 1	Bits 00…15 (00…17)	**Channel 0 output data** – The output data is real-time data that is formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 2	Bits 00…15 (00…17)	**Channel 1 output data** – The output data is real-time data that is formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 3	Bits 00…15 (00…17)	**Channel 2 output data** – The output data is real-time data that is formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 4	Bits 00…15 (00…17)	**Channel 4 output data** – The output data is real-time data that is formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 5	Channel Configuration	
	Bits 00…03	Channel 0 Configuration
	Bits 04…07	Channel 1 Configuration
	Bits 08…11 (10…13)	Channel 2 Configuration
	Bits 12…15 (14…17)	Channel 3 Configuration
Word 6	Bits 00…03	**Channel calibration selection bit** – When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, it 02 corresponds to input channel 2, bit 03 corresponds to input channel 3.
	Bit 04	**Gain/Offset selection bit (G0)** – When this bit is cleared, a 0…1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK)** – When this bit is set to 1 (calibration mode), the calibration coefficient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for successful calibration.
	Bit 06	**Quick Calibration bit (QK)** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **Note:** This method of calibration quickly calibrates the selected channels, however you are not within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV)** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **Note:** You are not within the rated accuracy of the module.
	Bits 08…11 (10…13)	**Request for hold outputs (Q)** – Channel request bits that instruct an output to hold its output level when EN transitions from 1 to 0 to 1. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs hold their level until the output data equals the output level. P0…P3 indicates channels holding. Output readback data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 08 (10) = channel 1, and so on.
	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5 ms update rate are reduced to 5.0 ms. When reset (0), real-time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR)** – This bit, when set to 1, permits configuration to be changed without using the IC bit.

Table 29 - Word/Bit Descriptions for 1794-OF4I Isolated Analog Output Module (Continued)

Word	Decimal Bit (Octal Bit)	Definition
Word 6	Bit 14 (16)	Set to 1
	Bit 15 (17)	**Initiate Configuration bit (IC)** – When set (1), instructs the module to enter configuration mode. Present configuration data before or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subsequent configuration information is ignored until IC is toggled.
Words 7	Bits 00...15 (00...17)	Not used

Isolated Analog Combo Module — 1794-IF2X0F2I Series B Image Table Mapping

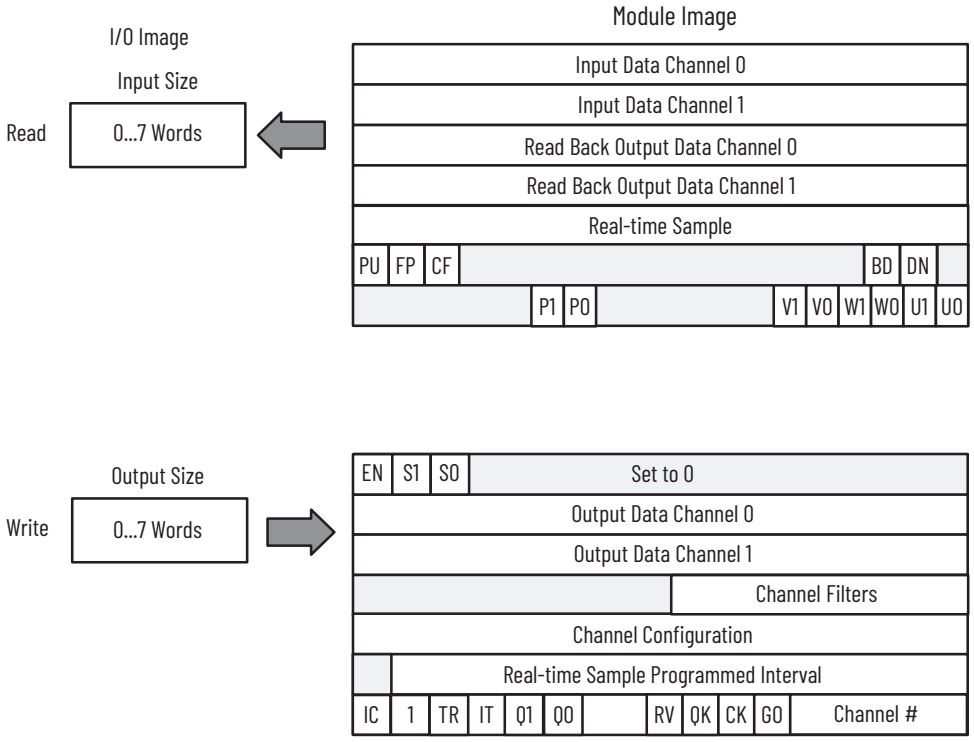


Table 30 - Analog Combo Module — 1794-IF2X0F2I Read

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 0	Input Data Channel 0															
Word 1	Input Data Channel 1															
Word 2	Read Back Channel 0															
Word 3	Read Back Channel 1															
Word 4	0	Real-time Sample														
Word 5	PU	FP	CF	0	Reserved				0	0	0	0	0	BD	DN	0
Word 6	0	0	0	0	P1	P0	0	0	0	0	V1	V0	W1	W0	U1	U0

Where:
PU = Power-up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
P0 and P1 = Output holding in response to Q0...Q1
W0 and W1 = Wire off current loop status for input channels 0 and 1 respectively. Not used on voltage outputs.
U0 and U1 = Underrange for input channels 0 and 1 respectively
V0 and V1 = Overrange for input channels 0 and 1 respectively

Table 31 - Configure Your Input Channels

Input Channel Configuration										
03	02	01	00	Set these bits for Channel 0						
07	06	05	04	Set these bits for Channel 1						
Bit Settings				**Input Values**	**Data Format**	**% Underrange % Overrange**	**Input Range[1]**		**Module Update Rate**	
							Hexadecimal	**Decimal**	**(RTSI = 0)**	**(RTSI = 0) IT = 1**
0	0	0	0	Channel not configured						
0	0	0	1	4...20 mA	Signed 2's complement	4% Under; 4% Over	<0000...7878>	<0000...30840>	7.5 ms	5.0 ms
0	0	1	0	±10V	Signed 2's complement	2% Under; 2% Over	<831F...7CE1>	<-31969...31969>	2.5 ms	2.5 ms
0	0	1	1	±5V	Signed 2's complement	4% Under; 4% Over	<8618...79E8>	<-31208...31208>	2.5 ms	2.5 ms
0	1	0	0	0...20 mA	Signed 2's complement %	0% Under; 4% Over	<0...2710>	<0...10000>	7.5 ms	5.0 ms
0	1	0	1	4...20 mA	Signed 2's complement %	4% Under; 4% Over	<0...2710>	<0...10000>	7.5 ms	5.0 ms
0	1	1	0	0...10V	Signed 2's complement %	0% Under; 2% Over	<0...2710>	<0...10000>	5.0 ms	5.0 ms
0	1	1	1	±10V	Signed 2's complement %	2% Under; 2% Over	<D8F0...2710>	<-10000...10000>	5.0 ms	5.0 ms
1	0	0	0	0...20 mA	Binary	0% Under; 4% Over	<0000...F3CF>	<0000...62415>	2.5 ms	2.5 ms
1	0	0	1	4...20 mA[2]	Binary	4% Under; 4% Over	<0000...F0F1>	<0000...61681>	7.5 ms	5.0 ms
1	0	1	0	0...10V	Binary	0% Under; 2% Over	<0000...F9C2>	<0000...63938>	2.5 ms	2.5 ms
1	0	1	1	0...5V	Binary	0% Under; 4% Over	<0000...F3CF>	<0000...62415>	2.5 ms	2.5 ms
1	1	0	0	0...20 mA	Offset binary, 8000 H = 0 mA	4% Under; 4% Over	<0618...F9E8>	<1560...63976>	2.5 ms	2.5 ms
1	1	0	1	4...20 mA	Offset binary, 8000 H = 4 mA	4% Under; 4% Over	<8000...F878>	<32768...63608>	7.5 ms	5.0 ms
1	1	1	0	±10V	Offset binary, 8000 H = 0 mA	2% Under; 2% Over	<031F...FCE1>	<799...64737>	2.5 ms	2.5 ms
1	1	1	1	±5V	Offset binary, 8000 H = 0 mA	4% Under; 4% Over	<0618...F9E8>	<1560...63976>	2.5 ms	2.5 ms

(1) < and > indicate the overrun beyond the actual range (about 5%).
(2) Underrange for 4...20 mA occurs in the blind area below 0 (3.2 mA).

Table 32 - Set Input Filter

Bits				Channel	
03	02	01	00	Input Channel 0	
07	06	05	04	Input Channel 1	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200 Hz	No low pass
0	0	0	1	1200 Hz	100 ms low pass
0	0	1	0	1200 Hz	500 ms low pass
0	0	1	1	1200 Hz	1000 ms low pass
0	1	0	0	600 Hz	No low pass
0	1	0	1	600 Hz	100 ms low pass
0	1	1	0	600 Hz	500 ms low pass
0	1	1	1	600 Hz	1000 ms low pass
1	0	0	0	300 Hz	No low pass
1	0	0	1	300 Hz	100 ms low pass
1	0	1	0	300 Hz	500 ms low pass
1	0	1	1	300 Hz	1000 ms low pass
1	1	0	0	150 Hz	No low pass
1	1	0	1	150 Hz	100 ms low pass
1	1	1	0	150 Hz	500 ms low pass
1	1	1	1	150 Hz	1000 ms low pass

Table 33 - Configure Your Outputs for the 1794-IF2XOF2I Analog Combo Module

Configuration Bits				Nominal Range	Data Type	Output Values[1]		Update Rate
MSD		LSD				Hexadecimal	Decimal	
0	0	0	1	4...20 mA	Signed 2's complement	<0000...7878>	<0000...30840>	5.0 ms
0	0	1	0	±10V	Signed 2's complement	<8618...79E8>	<-31208...31208>	2.5 ms
0	0	1	1	±5V	Signed 2's complement	<8618...79E8>	<-31208...31208>	2.5 ms
0	1	0	0	0...20 mA	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	0	1	4...20 mA	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	1	0	0...10V	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	1	1	±10V	Signed 2's complement %	<D8F0...2710>	<-10000...10000>	5.0 ms
1	0	0	0	0...20 mA	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	0	1	4...20 mA	Binary	<0000...F0F1>	<0000...61681>	5.0 ms
1	0	1	0	0...10V	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	1	1	0...5V	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	1	0	0	0...20 mA	Offset binary	<8000...F9E8>	<32768...63976>	2.5 ms
1	1	0	1	4...20 mA	Offset binary	<8000...F878>	<32768...63608>	5.0 ms
1	1	1	0	±10V	Offset binary	<0618...F9E8>	<1560...63976>	2.5 ms
1	1	1	1	±5V	Offset binary	<0618...F9E8>	<1560...63976>	2.5 ms

(1) < and > indicate the overrun beyond the actual range (about 5%).

Table 34 - Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module

Write Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00...15 (00...17)	**Input Channel 0 input data** – 16-bit unipolar; 15-bit plus sign bipolar
Word 1	Bits 00...15 (00...17)	**Input Channel 1 input data** – 16-bit unipolar; 15-bit plus sign bipolar
Word 2	Bits 00...15 (00...17)	**Read Back Output Channel 0** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0.
Word 3	Bits 00...15 (00...17)	**Read Back Output Channel 1** – During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0.
Word 4	Bits 00...15 (00...17)	**Real-time Sample** – The fixed time period that you set tells the module when to provide data to the processor.
Word 5	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN)** – This bit is set to 1 after a calibration cycle is completed.
	Bits 02	**Calibration Bad bit (BD)** – This bit is set to 1 if the channel calibration coefficients cannot be saved or read properly.
	Bits 03...07	Set to 0
	Bits 08...11 (10...12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the configuration mode is selected (bit 15, word 6 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU)** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 6	Bits 00...01	**Underrange bits (U)** – These bits, when set (1), indicate that the corresponding current output channel is open. W0 (bit 02) corresponds to channel 0, and W1 (bit 03) corresponds to channel 1.
	Bits 02...03	**Wire-Off status bits. (W)** – These bits, when set (1), indicate that the corresponding current output channel is open. W0 corresponds to channel 0, W1 corresponds to channel 2, and so on.
	Bits 04...05	**Overrange bits (V)** – These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1.
	Bits 06...09 (06...11)	Not used. Set to 0.
	Bits 10...11 (12...13)	**Hold output bits (P)** – These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12...15 (14...17)	Not used. Set to 0.

Table 34 - Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module (Continued)

Write Word	Decimal Bit (Octal Bit)	Definition
Write Word 0	Bits 00…12 (00…14)	Not used
	Bits 13…14 (15…16)	**Safe State Source bits (S1/S0)** – When EN is 0, these bits designate the source of the safe state data. Bit 13 = 0; Bit 14 = 1 – reset outputs to 0V/0 mA Bit 13 = 1; Bit 14 = 1 – hold output at its current level
	Bits 15 (17)	**Output enable bit (EN)** – When set (1), the outputs are enabled. This bit must be set in order for the real-time data to appear at the outputs. If this bit is not set (0), then S1/S0 determines the outputs.
Word 1	Bits 00…15 (00…17)	**Output Channel 0 data**
Word 2	Bits 00…15 (00…17)	**Output Channel 1 data**
Word 3	**Input Channels 0 and 1 Filter Selections**	
	Bits 00…01	Channel 0 Filter Setting
	Bits 04…07	Channel 1 Filter Setting
	Bits 08…15 (10…17)	Set to 0
Word 4	**Channel Configuration**	
	Bit 00…03	**Input Channel 0 Configuration**
	Bits 04…07	**Input Channel 1 Configuration**
	Bits 08…11 (10…13)	**Output Channel 0 Configuration**
	Bits 12…15 (14…17)	**Output Channel 1 Configuration**
Word 5	Bits 00…14 (00…16)	**Real-time Sample Interval** – Programs the interval of the real-time sample. Can be varied from 0…30 seconds (30,000 decimal). Resolution is in ms with granularity in 5 ms steps.
	Bit 15 (17)	Set to 0
Word 6	Bits 00…03	**Channel calibration selection bit** – When this bit is set (1), the channel can be calibrated using the initiate calibration bit (IC). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, bit 02 corresponds to output channel 0, bit 03 corresponds to output channel 1.
	Bit 04	**Gain/Offset selection bit (GO)** – When this bit is set (1), a reset (0), set (1), reset (0) pattern of the calibration clock bit (CK) causes a gain calibration to occur. When this bit is set to 0, a reset (0), set (1), reset (0) pattern of the calibration clock bit (CK) causes an offset calibration to occur.
	Bit 05	**Calibration clock bit (CK)** – When this bit is set to 1 (calibration mode), the calibration coefficient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients are stored in the selected channels, applied, and the calibration mode exited. Monitor status bits DN and BD for successful calibration.
	Bit 06	**Quick Calibration bit (QK)** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **Note:** This method of calibration quickly calibrates the selected channels, you are not within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV)** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient.
	Bits 08…09 (10…11)	Not used. Set to 0.
	Bits 10…11 (12…13)	**Request for hold outputs (Q)** – Channel request bits that instruct an output to hold its output level when EN transitions from 0 to 1 to 0. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs hold their level until the output data equals the output level. P0…P3 indicates channels holding. Output readback data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 08 (10) = channel 1, and so on.
	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5 ms update rate are reduced to 5.0 ms. When reset (0), real-time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR)** – This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 14 (16)	Set to 1
	Bit 15 (17)	**Initiate Configuration bit (IC)** – When set (1), instructs the module to enter configuration mode. Present configuration data before or coincident with IC being set. Once IC returns to 0, additional configuration information is ignored.
Word 7	Bits 00…15 (00…17)	Not used

Defaults

Each I/O module has default values that are associated with it. At default, each module generates inputs/status and expects outputs/configuration.

Module Defaults for:		Factory Defaults		Real-time Size	
Catalog Number	Description	Input Default	Output Defaults	Input Defaults	Output Defaults
1794-IF4I	4-pt Isolated Analog Input	7	8	4	0
1794-OF4I	4-pt Isolated Analog Output	6	9	4	5
1794-IF2XOF2I	2 in/2 out Isolated Analog Combo	7	8	4	2

Factory defaults are the values available by the adapter.

You can change the I/O data size for a module by reducing the number of words that are mapped into the adapter, as shown in real-time sizes.

Real-time sizes are the settings that provide optimal real-time data to the adapter. These values appear when you:

- First power up the system, and
- No previous stored settings have been applied.

Analog modules have 15 words that are assigned to them. These words are divided into input words/output words. You can reduce the I/O data size to fewer words to increase data transfer over the backplane. For example, a 4 input analog module has 7 words input/8 words output. You can reduce the input words to 4 by not using the real-time sample, module status, or channel status. Likewise, you can reduce the write words to 0, thus removing the conversion rate/filter settings, channel range/data format, real-time sample interval and configuration/calibration, and unused words.

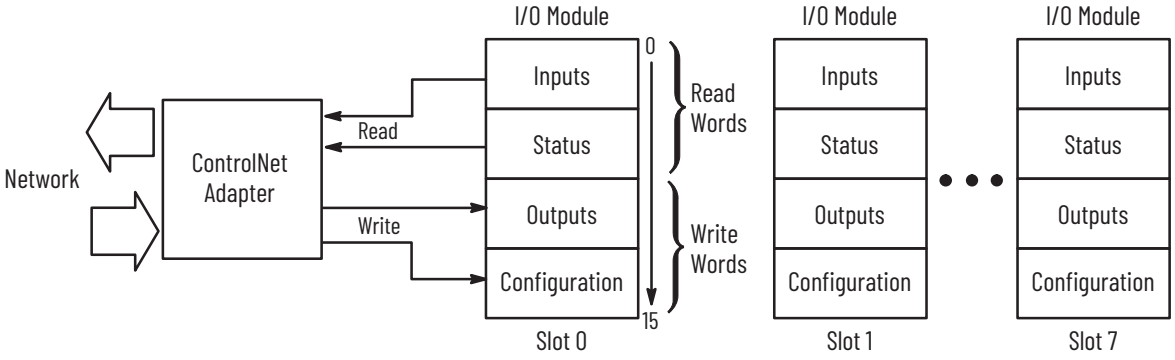
Input, Output, Status, and Configuration Files for Analog Modules when used with ControlNet

About the ControlNet Adapter

The FLEX I/O ControlNet adapter, catalog numbers 1794-ACN15 and 1794-ACNR15, is the interface between up to eight FLEX I/O modules and a ControlNet processor or scanner. The adapter can support ControlNet real-time data connections to individual modules or module groups. Each connection is independent of the others and can be from different processors or scanners.

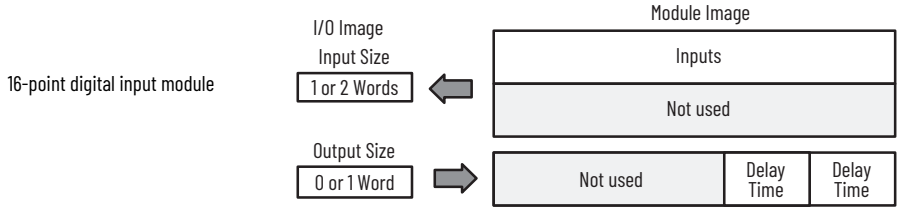
Communication Over the FLEX I/O Backplane

One 1794-ACN15 and 1794-ACNR15 ControlNet adapter can interface with up to eight terminal base units with installed FLEX I/O modules, to form a FLEX I/O system of up to eight slots. The adapter communicates to other network system components (typically one or more controllers or scanners, and/or programming terminals) over the DeviceNet network. The adapter communicates with its I/O modules over the backplane.



The I/O map for a module is divided into read words and write words. Read words consist of input and status words, and write words consist of output and configuration words. The number of read words or write words can be 0 or more. The length of each I/O module's read words and write words vary in size depending on module complexity. Each I/O module supports at least 1 input word or 1 output word. Status and configuration are optional, depending on the module.

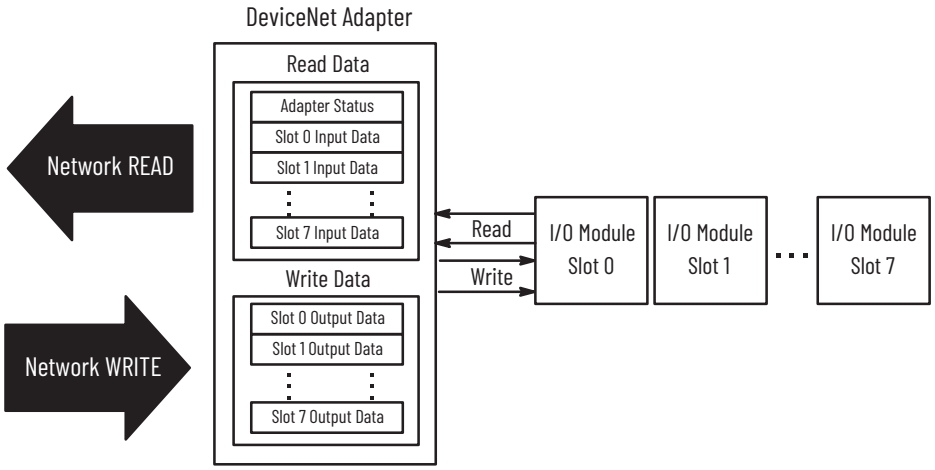
For example, a 16-point digital input module has up to 2 read words and 1 write word.



Polled I/O Structure

The adapter receives the output data in the order of the installed I/O modules. The output data for slot 0 is received first, followed by the output data for slot 1, and so on, up to slot 7.

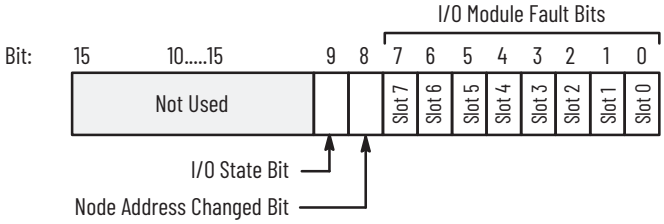
The first word of input data that the adapter sends is the Adapter Status Word. This is followed by the input data from each slot, in the order of the installed I/O modules. The input data from slot 0 is first after the status word, followed by input data from slot 2, and so on, up to slot 7.



Adapter Input Status Word

The input status word consists of:

- I/O module fault bits – 1 status bit for each slot
- Node address changed – 1 bit
- I/O status – 1 bit



The adapter input status word bit descriptions are shown in the following table.

Bit Description	Bit	Explanation
I/O Module Faults	0	This bit is set (1) when an error is detected in slot position 0.
	1	This bit is set (1) when an error is detected in slot position 1.
	2	This bit is set (1) when an error is detected in slot position 2.
	3	This bit is set (1) when an error is detected in slot position 3.
	4	This bit is set (1) when an error is detected in slot position 4.
	5	This bit is set (1) when an error is detected in slot position 5.
	6	This bit is set (1) when an error is detected in slot position 6.
	7	This bit is set (1) when an error is detected in slot position 7.
Node Address Changed	8	This bit is set (1) when the node address switch setting has been changed since power-up.
I/O Status	9	Bit = 0 – idle Bit = 1 – run
—	10...15	Not used – sent as zeros

Possible causes for an **I/O Module Fault** are:

- Transmission errors on the FLEX I/O backplane
- A failed module
- A module removed from its terminal base
- Incorrect module insertion in a slot position
- The slot is empty

Safe State Data

The ControlNet adapter provides the non-discrete module output data during communication faults or processor idle state. This "safe state data" verifies that a known output is applied to the output devices to maintain a previously designated safe operating condition during the previously mentioned failure modes. The processor or scanner software must include the means to specify this safe state data for each non-discrete module.

Communication Fault Behavior

You can configure the adapter response to a communication fault for each I/O module in its system. Upon detection of a communication fault, the adapter can:

- Leave the module output data in its last state (hold last state)
- Reset the module output data to zero (reset)
- Apply safe state data to the module output

Idle State Behavior

The ControlNet adapter can detect the state of the controlling processor or scanner. Only 2 states can be detected: run mode, or program mode (idle).

When run mode is detected, the adapter copies the output data that is received from the processor to the corresponding module output. When program mode is detected, the adapter can be configured to:

- Leave the module output data in its last state (hold last state)
- Reset the module output data to zero (reset)
- Apply safe state data to the module output

Input Data Behavior Upon Module Removal

I/O module input data that the adapter sends upon module removal is configurable. The adapter can:

- Reset the module output data to zero (reset)
- Leave the module output data in the last state before module removal (hold last state)

To find the image table for:	See page
4 Input Isolated Analog Module — 1794-IF4I, 1794-IF4IXT, 1794-IF4ICFXT Table Mapping	60
4 Isolated Output Analog Module — 1794-OF4I Image Table Mapping	63
Isolated Analog Combo Module — 1794-IF2XOF2I Image Table Mapping	66

4 Input Isolated Analog Module — 1794-IF4I, 1794-IF4IXT, 1794-IF4ICFXT Table Mapping

Set EN bit Off (0) for the Configuration block. Module actions (Reset, Safe State and Hold Last State) are set using programming software.

Table 35 - Input Map

Dec.	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Oct.	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 0	Analog Value Channel 0															
Word 1	Analog Value Channel 1															
Word 2	Analog Value Channel 2															
Word 3	Analog Value Channel 3															
Word 4	Real-time Sample															
Word 5	PU	FP	CF	0	Reserved				0	0	0	0	0	BD	DN	0
Word 6	0	0	0	0	0	0	0	0	V3	V2	V1	V0	U3	U2	U1	U0

Where:
PU = Power-up unconfigured
FP = Field power off
CF = In configuration mode
BD = Bad calibration
DN = Calibration accepted
U = Underrange for specified channel
V = Overrange for specified channel

Table 36 - Output (Configuration) Map

Dec.	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Oct.	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 0	PU	FP	CF	0	Reserved				0	0	0	0	0	BD	DN	0
Word 1	Ch 3 Filter				Ch 2 Filter				Ch 1 Filter				Ch 0 Filter			
Word 2	Output Ch 3 Configuration				Output Ch 2 Configuration				Output Ch 1 Configuration				Output Ch 0 Configuration			
Word 3	0	Real-time Sample Interval														
Word 4	IC	1	TR	IT	0	CH	SK	FS	RV	QK	CK	GO	Channel Number			
Word 5	Reserved															

Where:
EN = Enable bit (not used on input module)
IC = Initiate Configuration bit
TR = Transparent bit
IT = Interrupt toggle bit
CH - Chop Mode Disable
SK = FIR Filter Disable
FS = Fast Step Response
RV = Revert to default bit
QK = Quick calibration
CK = Calibration clock
GO = Gain Offset select

Table 37 - Word/Bit Descriptions for Isolated Analog Input Module

Word	Decimal Bit (Octal Bit)	Definition
Input Words		
Word 0	Bits 00...15 (00...17)	**Channel 0 analog data** – Real-time input data per your configuration
Word 1	Bits 00...15 (00...17)	**Channel 1 analog data** – Real-time input data per your configuration
Word 2	Bits 00...15 (00...17)	**Channel 2 analog data** – Real-time input data per your configuration
Word 3	Bits 00...15(00...17)	**Channel 3 analog data** – Real-time input data per your configuration
Word 4	Bits 00...15 (00...17)	**Real-time Sample** – The elapsed time in increments programmed by the real-time sample interval.
Word 5	Bit 00	Reserved
	Bit 01	**Calibration Done bit (DN)** – This bit is set to 1 after a calibration cycle is completed.
	Bit 02	**Calibration Bad bit (BD)** – This bit is set to 1 if the channel calibration coefficients cannot be saved or be read properly.
	Bits 03...07	Set to 0
	Bits 08...11 (10...13)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the calibration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.

Table 37 - Word/Bit Descriptions for Isolated Analog Input Module (Continued)

Word	Decimal Bit (Octal Bit)	Definition
Word 5	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU)** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 6	Bits 00…03	**Underrange bits (U)** – These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, and so on.
	Bits 04…07	**Overrange bits (V)** – These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1, and so on.
	Bits 08…15 (10…17)	Not used. Set to 0.
Configuration Words		
Word 0	Bits 00…14 (00…16)	Not used. Set to 0.
	Bit 15 (17)	**Output enable bit (EN)** – Not used in the 1794-IF4I module
Word 1	**Channels 0…3 Filter Selections**	
	Bits 00…03	Channel 0 Filter Setting
	Bits 04…07	Channel 1 Filter Setting
	Bits 08…11 (00…13)	Channel 2 Filter Setting
	Bits 12…15 (14…17)	Channel 3 Filter Setting
Word 2	**Channel Configuration**	
	Bits 00…03	Channel 0 Configuration
	Bits 04…07	Channel 1 Configuration
	Bits 08…11(10…13)	Channel 2 Configuration
	Bits 12…15 (14…17)	Channel 3 Configuration
Word 3	Bits 00…14 (00…16)	**Real-time Sample Interval** – Programs the interval of the real-time sample. Can be varied 0…30 seconds (30,000 decimal). Resolution is in ms with granularity in 5 ms steps.
	Bit 15 (17)	Not used. Set to 0.
Word 4	Bits 00…03	**Channel calibration selection bit** – When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, it 02 corresponds to input channel 2, bit 03 corresponds to input channel 3.
	Bit 04	**Gain/Offset selection bit (GO)** – When this bit is cleared, a 0…1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK)** – When this bit is set to 1 (calibration mode), the calibration coefficient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for successful calibration.
	Bit 06	**Quick Calibration bit (QK)** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **Note:** This method of calibration quickly calibrates the selected channels, however you are not within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV)** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **Note:** You are not within the rated accuracy of the module.
	Bits 08	**1794-IF4I** – Not used. Set to 0. **1794-IF4ICFXT** – **FastStepResponse (FR) –** Use to enable a fast step response algorithm. The fast step response algorithm, upon sensing a step input, uses an averaging method rather than the FIR filter. The FIR returns to operation once the input has settled. The default is fast step response disabled (0).
	Bit 09	**1794-IF4I** - Not used. Set to 0. **1794-IF4ICFXT** – **FIR Filter Disable (SK)** - Use to disable the FIR filter. The Finite Impulse Response filter is used by the module to improve signal stability. The default is FIR filter enabled (0).
	Bit 10	**1794-IF4I** - Not used. Set to 0. **1794-IF4ICFXT** – **Chop Mode Disable (CH)** – Use to disable the chop mode. Chop mode used by the module to reduce offset and drift errors. The default is chop mode enabled (0).
	Bit 11	Not used. Set to 0.

Table 37 - Word/Bit Descriptions for Isolated Analog Input Module (Continued)

Word	Decimal Bit (Octal Bit)	Definition
Word 4	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5 ms update rate are reduced to 5.0 ms. When reset (0), real-time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR)** – This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 14 (16)	Set to 1
	Bit 15 (17)	**Initiate Configuration bit (IC)** – When set (1), instructs the module to enter configuration mode. Present configuration data before or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subsequent configuration information is ignored until IC is toggled.

Table 38 - Set Input Filter

Bits				Channel	
03	02	01	00	Input 0	
07	06	05	04	Input 1	
11	10	09	08	Input 2	
15	014	13	12	Input 3	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200 Hz	No low pass
0	0	0	1	1200 Hz	100 ms low pass
0	0	1	0	1200 Hz	500 ms low pass
0	0	1	1	1200 Hz	1000 ms low pass
0	1	0	0	600 Hz	No low pass
0	1	0	1	600 Hz	100 ms low pass
0	1	1	0	600 Hz	500 ms low pass
0	1	1	1	600 Hz	1000 ms low pass
1	0	0	0	300 Hz	No low pass
1	0	0	1	300 Hz	100 ms low pass
1	0	1	0	300 Hz	500 ms low pass
1	0	1	1	300 Hz	1000 ms low pass
1	1	0	0	150 Hz	No low pass
1	1	0	1	150 Hz	100 ms low pass
1	1	1	0	150 Hz	500 ms low pass
1	1	1	1	150 Hz	1000 ms low pass

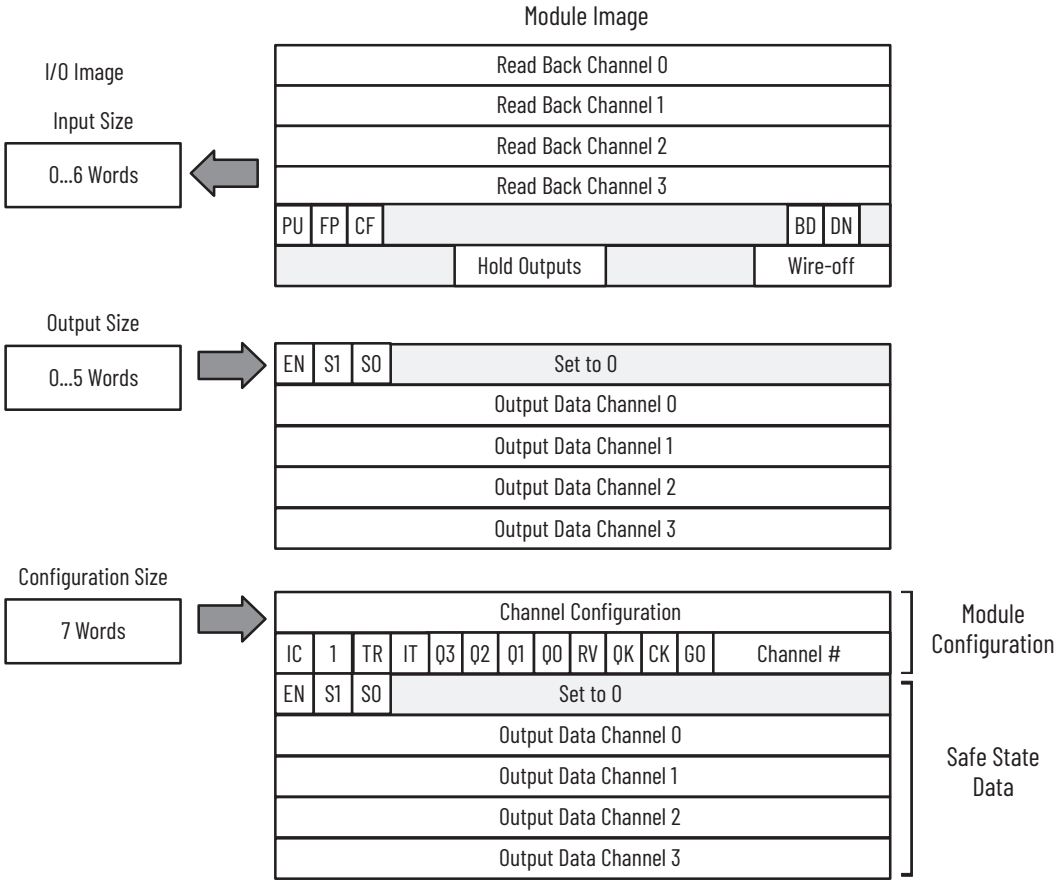
Table 39 - Configure Your Input Module

Input Channel Configuration									
03	02	01	00	Set these bits for Channel 0					
07	06	05	04	Set these bits for Channel 1					
11	10	09	08	Set these bits for Channel 2					
15	14	13	12	Set these bits for Channel 3					
Bit Settings				**Input Values**	**Data Format**	**% Underrange % Overrange**	**Input Range**		**Module Update Rate**
							Hexadecimal	**Decimal**	**(RTSI = 0)**
0	0	0	0	Channel not configured					
0	0	0	1	4...20 mA	Signed 2's complement	4% Under; 4% Over	<0000...7878>	<0000...30840>	7.5 ms
0	0	1	0	±10V	Signed 2's complement	2% Under; 2% Over	<831F...7CE1>	<-31969...31969>	2.5 ms
0	0	1	1	±5V	Signed 2's complement	4% Under; 4% Over	<8618...79E8>	<-31208...31208>	2.5 ms
0	1	0	0	0...20 mA	Signed 2's complement %	0% Under; 4% Over	<0...2710>	<0...10000>	7.5 ms
0	1	0	1	4...20 mA	Signed 2's complement %	4% Under; 4% Over	<0...2710>	<0...10000>	7.5 ms
0	1	1	0	0...10V	Signed 2's complement %	0% Under; 2% Over	<0...2710>	<0...10000>	5.0 ms

Table 39 - Configure Your Input Module (Continued)

Input Channel Configuration									
0	1	1	1	±10V	Signed 2's complement %	2% Under; 2% Over	<D8F0...2710>	<-10000...10000>	5.0 ms
1	0	0	0	0...20 mA	Binary	0% Under; 4% Over	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	0	1	4...20 mA	Binary	4% Under; 4% Over	<0000...F0F1>	<0000...61684>	7.5 ms
1	0	1	0	0...10V	Binary	0% Under; 2% Over	<0000...F9C2>	<0000...63938>	2.5 ms
1	0	1	1	0...5V	Binary	0% Under; 4% Over	<0000...F3CF>	<0000...62415>	2.5 ms
1	1	0	0	0...20 mA	Offset binary, 8000 H = 0 mA	4% Under; 4% Over	<0618...F9E8>	<1560...63976>	2.5 ms
1	1	0	1	4...20 mA	Offset binary, 8000 H = 4 mA	4% Under; 4% Over	<8000...F878>	<32768...63608>	7.5 ms
1	1	1	0	±10V	Offset binary, 8000 H = 0 mA	2% Under; 2% Over	<031F...FCE1>	<799...64737>	2.5 ms
1	1	1	1	±5V	Offset binary, 8000 H = 0 mA	4% Under; 4% Over	<0618...F9E8>	<1560...63976>	2.5 ms

4 Isolated Output Analog Module — 1794-OF4I Image Table Mapping



Set EN bit Off (0) for the Configuration block.
Set EN bit On (1) for the Output block.
S0 and S1 bits are not used in ControlNet applications. Set to Off (0).
Module actions (Reset, Safe State, and Hold Last State) are set using programming software.

Table 40 - Word/Bit Descriptions for the 1794-OF4I Analog Output Module

Word	Decimal Bit (Octal Bit)	Definition
Input Words		
Word 0	Bits 00...15 (00...17)	**Read Back Channel 0** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 1	Bits 00...15 (00...17)	**Read Back Channel 1** – During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.

Table 40 - Word/Bit Descriptions for the 1794-OF4I Analog Output Module (Continued)

Word	Decimal Bit (Octal Bit)	Definition
Word 2	Bits 00…15 (00…17)	**Read Back Channel 2** – During normal operation, it is a copy of the output of channel 2. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 3	Bits 00…15 (00…17)	**Read Back Channel 3** – During normal operation, it is a copy of the output of channel 3. During an EN transition, it is the condition of the output as determined by S1 and S0. Readback is an image of what you have sent as output to the module; no checks are performed on the data.
Word 4	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN)** – This bit is set to 1 after a calibration cycle is completed.
	Bits 02	**Calibration Bad bit (BD)** – This bit is set to 1 if the channel calibration coefficients cannot be saved or read properly.
	Bits 03…07	Set to 0
	Bits 08…11 (10…12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the configuration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set, the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU)** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set, the module status indicator flashes.
Word 5	Bits 00…03	**Wire-Off status bits. (W)** – These bits, when set (1), indicate that the corresponding current output channel is open. W0 corresponds to channel 0, W1 corresponds to channel 2, and so on.
	Bits 04…07	Set to 0
	Bits 10…11 (12…13)	**Hold output bits (P)** – These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12…15 (14…17)	Set to 0
Output Words		
Word 0	Bits 00…12 (00…14)	Not used
	Bits 13…14 (15…16)	**Safe State Source bits (S1/S0)** – Not used in ControlNet applications. Turn off these bits (set to 0).
	Bits 15 (17)	**Output enable bit (EN)** – Set this bit off (0) for the configuration block. Set this bit on (1) for the output block.
Word 1	Bits 00…15 (00…17)	**Channel 0 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 2	Bits 00…15 (00…17)	**Channel 1 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 3	Bits 00…15 (00…17)	**Channel 2 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 4	Bits 00…15 (00…17)	**Channel 3 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Configuration Words		
Word 0	**Channel Configuration**	
	Bits 00…03	Channel 0 Configuration
	Bits 04…07	Channel 1 Configuration
	Bits 08…11 (10…13)	Channel 2 Configuration
	Bits 12…15 (14…17)	Channel 3 Configuration
Word 1	Bits 00…03	**Channel calibration selection bit** – When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to output channel 0, bit 01 corresponds to output channel 1, it 02 corresponds to output channel 3, bit 03 corresponds to output channel 4.
	Bit 04	**Gain/Offset selection bit (GO)** – When this bit is cleared, a 0…1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK)** – When this bit is set to 1 (calibration mode), the calibration coefficient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for successful calibration.
	Bit 06	**Quick Calibration bit (QK)** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **Note:** Although this method of calibration quickly calibrates the selected channels, they are not within the rated accuracy of the module.

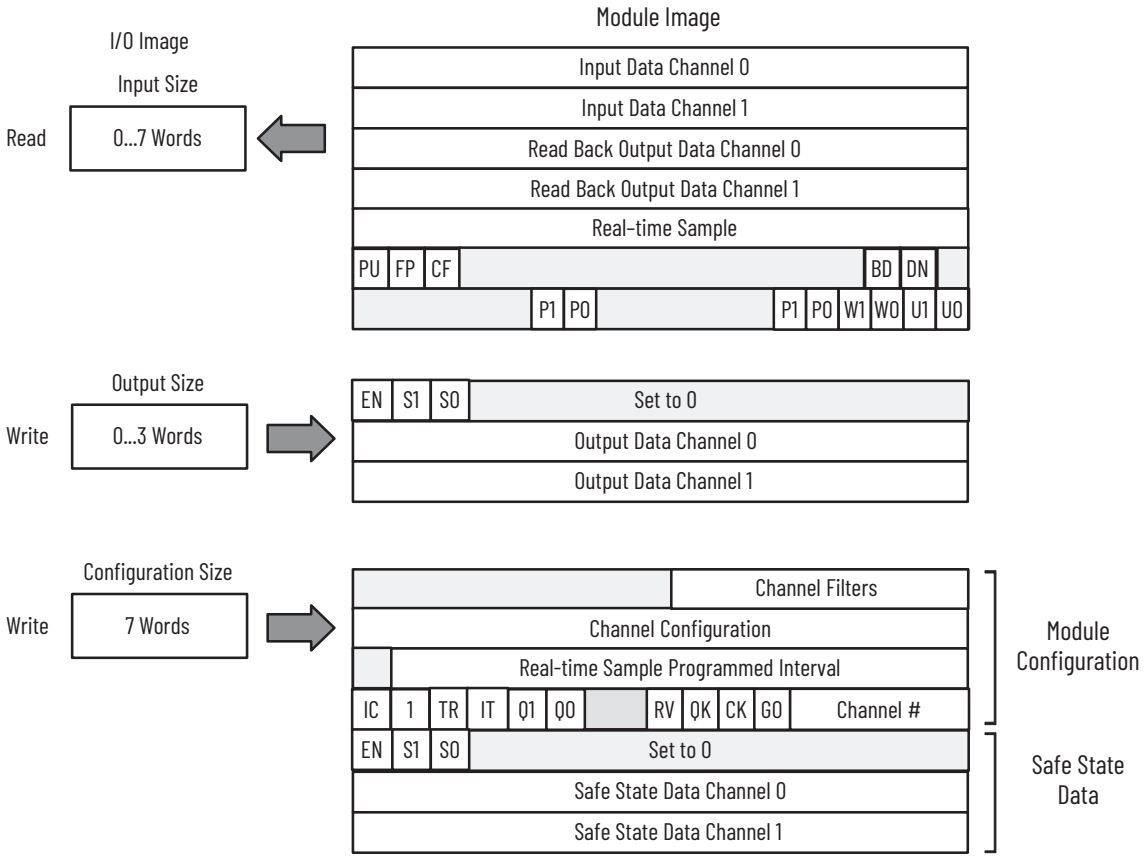
Table 40 - Word/Bit Descriptions for the 1794-OF4I Analog Output Module (Continued)

Word	Decimal Bit (Octal Bit)	Definition
Word 1	Bit 07	**Revert to defaults bit (RV)** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **Note:** They are not within the rated accuracy of the module.
	Bits 08...11 (10...13)	**Request for hold outputs (Q)** – Channel request bits that instruct an output to hold its output level when EN transitions from 1 to 0 to 1. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs hold their level until the output data equals the output level. P0–P3 indicates channels holding. Output readback data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 09 (11) = channel 1, and so on.
	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5 ms update rate are reduced to 5.0 ms. When reset (0), real-time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR)** – This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 14 (16)	Set to 1
	Bit 15 (17)	**Initiate Configuration bit (IC)** – When set (1), instructs the module to enter configuration mode. Present configuration data before or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subsequent configuration information is ignored until IC is toggled.
Word 2	Bits 00...12 (00...14)	Not used
	Bits 13...14 (15...16)	**Safe State Source bits (S1/S0)** – When EN is 0, these bits designate the source of the safe state data. Bit 13 = 0, bit 14 = 1 – reset outputs to 0V/0mA (used with 1794-ASB/C) Bit 13 = 1, bit 14 = 1 – hold output at its current level (used with 1794-ASB/C) Bit 13 = 0; bit 14 = 0 – Safe state data is in output data words
	Bits 15 (17)	**Output enable bit (EN)** – When set (1), the outputs are enabled. This bit must be set in order for the real-time data to appear at the outputs. If this bit is not set (0), then S1/S0 determines the outputs.
Word 3	Bits 00...15 (00...17)	**Channel 0 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 4	Bits 00...15 (00...17)	**Channel 1 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 5	Bits 00...15 (00...17)	**Channel 2 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 6	Bits 00...15 (00...17)	**Channel 3 output data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.

Table 41 - Configure Your Outputs – 1794-OF4I Isolated Output Module

Configuration Bits				Nominal Range	Data Type	Output Values		Update Rate
MSD		LSD				Hexadecimal	Decimal	
0	0	0	1	4...20 mA	Signed 2's complement	<0000...7878>	<0000...30840>	5.0 ms
0	0	1	0	±10V	Signed 2's complement	<8618...79E8>	<-31208...31208>	2.5 ms
0	0	1	1	±5V	Signed 2's complement	<8618...79E8>	<-31208...31208>	2.5 ms
0	1	0	0	0...20 mA	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	0	1	4...20 mA	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	1	0	0...10V	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	1	1	±10V	Signed 2's complement %	<D8F0...2710>	<-10000...10000>	5.0 ms
1	0	0	0	0...20 mA	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	0	1	4...20 mA	Binary	<0000...F0F1>	<0000...61681>	5.0 ms
1	0	1	0	0...10V	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	1	1	0...5V	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	1	0	0	0...20 mA	Offset binary	<8000...F9E8>	<32768...63976>	2.5 ms
1	1	0	1	4...20 mA	Offset binary	<8000...F878>	<32768...63608>	5.0 ms
1	1	1	0	±10V	Offset binary	<0618...F9E8>	<1560...63976>	2.5 ms
1	1	1	1	±5V	Offset binary	<0618...F9E8>	<1560...63976>	2.5 ms

Isolated Analog Combo Module — 1794-IF2X0F2I Image Table Mapping



Set EN bit Off (0) for the Configuration block.
Set EN bit On (1) for the Output block.
S0 and S1 bits are not used in ControlNet applications. Set to Off (0).
Module actions (Reset, Safe State, and Hold Last State) are set using programming software.

Table 42 - Word/Bit Descriptions for the 1794-IF2X0F2I Isolated Analog Combo Module

Write Word	Decimal Bit (Octal Bit)	Definition
Input Words		
Word 0	Bits 00...15 (00...17)	**Input Channel 0 input data** – Real-time input data per your configuration
Word 1	Bits 00...15 (00...17)	**Input Channel 1 input data** – Real-time input data per your configuration
Word 2	Bits 00...15 (00...17)	**Read Back Output Channel 0** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. **Note:** Readback data is an image of what you have sent as output to the module; no checks are performed on the data.
Word 3	Bits 00...15 (00...17)	**Read Back Output Channel 1** – During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0. **Note:** Readback data is an image of what you have sent as output to the module; no checks are performed on the data.
Word 4	Bits 00...15 (00...17)	**Real-time Sample** – The elapsed time in increments programmed by the real-time sample interval
Word 5	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN)** – This bit is set to 1 after a calibration cycle is completed.
	Bits 02	**Calibration Bad bit (BD)** – This bit is set to 1 if the channel calibration coefficients cannot be saved or read properly.
	Bits 03...07	Set to 0
	Bits 08...11 (10...12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the configuration mode is selected (bit 15, word 6 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.

Table 42 - Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module (Continued)

Write Word	Decimal Bit (Octal Bit)	Definition
Word 5	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU)** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 6	Bits 00…01	**Underrange bits (U)** – These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, and so on.
	Bits 02…03	**Wire-Off status bits. (W)** – These bits, when set (1), indicate that the corresponding current output channel is open. W0 corresponds to channel 0, W1 corresponds to channel 2, and so on.
	Bits 04…05	**Overrange bits (V)** – These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1.
	Bits 06…09 (06…11)	Not used. Set to 0.
	Bits 10…11 (12…13)	**Hold output bits (P)** – These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12…15 (14…17)	Not used. Set to 0.
Output Words		
Word 0	Bits 00…12 (00…14)	Not used
	Bits 13…14 (15…16)	**Safe State Source bits (S1/S0)** – When EN is 0, these bits designate the source of the safe state data. Bit 13 = 0; Bit 14 = 1 – reset outputs to 0V/0mA (used with 1794-ASB/C) Bit 13 = 1; Bit 14 = 1 – hold output at its current level (used with 1794-ASB/C) Bit 13 = 0; Bit 14 = 0 – Safe state data is in output data words
	Bits 15 (17)	**Output enable bit (EN)** – When set (1), the outputs are enabled. This bit must be set in order for the real-time data to appear at the outputs. If this bit is not set (0), then S1/S0 determines the outputs.
	Bits 00…15 (00…17)	**Output Channel 0 data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Word 1	Bits 00…15 (00…17)	**Output Channel 1 data** – The output data is real-time data that is formatted to the selected configuration. This data is also safe state data when directed by S1 and S0.
Configuration Words		
Word 0	**Input Channels 0 and 1 Filter Selections**	
	Bits 00…01	Channel 0 Filter Setting
	Bits 04…07	Channel 1 Filter Setting
	Bits 08…15 (10…17)	Not used
Word 1	**Channel Configuration**	
	Bits 00…03	**Input Channel 0 Configuration**
	Bits 04…07	**Input Channel 1 Configuration**
	Bits 08…11 (10…13)	**Output Channel 0 Configuration**
	Bits 12…15 (14…17)	**Output Channel 1 Configuration**
Word 2	Bits 00…14 (00…16)	**Real-time Sample Interval** – Programs the interval of the real-time sample. Can be varied 0…30 seconds (30,000 decimal). Resolution is in ms with granularity in 5 ms steps.
Word 3	Bits 00…03	**Channel calibration selection bit** – When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to output channel 0, bit 01 corresponds to output channel 1, bit 02 corresponds to output channel 3, bit 03 corresponds to output channel 4.
	Bit 04	**Gain/Offset selection bit (GO)** – When this bit is cleared, a 0…1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK)** – When this bit is set to 1 (calibration mode), the calibration coefficient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for successful calibration.
	Bit 06	**Quick Calibration bit (QK)** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **Note:** Although this method of calibration quickly calibrates the selected channels, they are not within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV)** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **Note:** They are not within the rated accuracy of the module.
	Bits 08…09 (10…11)	Not used. Set to 0.

Table 42 - Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module (Continued)

Write Word	Decimal Bit (Octal Bit)	Definition
Word 3	Bit 10…11 (12…13)	**Request for hold outputs (Q)** – Channel request bits that instruct an output to hold its output level when EN transitions from 1…0 to 1. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs hold their level until the output data equals the output level. P0–P3 indicates channels holding. Output readback data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 08 (10) = channel 1, and so on.
	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5 ms update rate are reduced to 5.0 ms. When reset (0), real-time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR)** – This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 15 (17)	**Initiate Configuration bit (IC)** – When set (1), instructs the module to enter configuration mode. Present configuration data before or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subsequent configuration information is ignored until IC is toggled.
Word 4	Bits 00…12 (00…14)	Not used
	Bits 13…14 (15…16)	**Safe State Source bits (S1/S0)** – Not used in ControlNet applications. Set these bits off (0).
	Bit 15 (17)	**Output enable bit (EN)** Set this bit off (0) for the configuration block. Set this bit on (1) for the output block.
Word 5	Bits 00…15 (00…17)	Output Channel 0 data
Word 6	Bits 00…15 (00…17)	Output Channel 1 data

Table 43 - Configure Your Input Channels

Input Channel Configuration									
03	02	01	00	Set these bits for Channel 0					
07	06	05	04	Set these bits for Channel 1					
Bit Settings				**Input Values**	**Data Format**	**% Underrange % Overrange**	**Input Range**		**Module Update Rate**
							Hexadecimal	**Decimal**	**(RTSI = 0)**
0	0	0	0	Channel not configured					
0	0	0	1	4…20 mA	Signed 2's complement	4% Under; 4% Over	<0000…7878>	<0000…30840>	7.5 ms
0	0	1	0	±10V	Signed 2's complement	2% Under; 2% Over	<831F…7CE1>	<-31969…31969>	2.5 ms
0	0	1	1	±5V	Signed 2's complement	4% Under; 4% Over	<8618…79E8>	<-31208…31208>	2.5 ms
0	1	0	0	0…20 mA	Signed 2's complement %	0% Under; 4% Over	<0…2710>	<0…10000>	7.5 ms
0	1	0	1	4…20 mA	Signed 2's complement %	4% Under; 4% Over	<0…2710>	<0…10000>	7.5 ms
0	1	1	0	0…10V	Signed 2's complement %	0% Under; 2% Over	<0…2710>	<0…10000>	5.0 ms
0	1	1	1	±10V	Signed 2's complement %	2% Under; 2% Over	<D8F0…2710>	<-10000…10000>	5.0 ms
1	0	0	0	0…20 mA	Binary	0% Under; 4% Over	<0000…F3CF>	<0000…62415>	2.5 ms
1	0	0	1	4…20 mA[1]	Binary	4% Under; 4% Over	<0000…F0F1>	<0000…61681>	7.5 ms
1	0	1	0	0…10V	Binary	0% Under; 2% Over	<0000…F9C2>	<0000…63938>	2.5 ms
1	0	1	1	0…5V	Binary	0% Under; 4% Over	<0000…F3CF>	<0000…62415>	2.5 ms
1	1	0	0	0…20 mA	Offset binary, 8000 H = 0 mA	4% Under; 4% Over	<0618…F9E8>	<1560…63976>	2.5 ms
1	1	0	1	4…20 mA	Offset binary, 8000 H = 4 mA	4% Under; 4% Over	<8000…F878>	<32768…63608>	7.5 ms
1	1	1	0	±10V	Offset binary, 8000 H = 0 mA	2% Under; 2% Over	<031F…FCE1>	<799…64737>	2.5 ms
1	1	1	1	±5V	Offset binary, 8000 H = 0 mA	4% Under; 4% Over	<0618…F9E8>	<1560…63976>	2.5 ms

(1) Underrange for 4…20 mA occurs in the blind area below 0 (3.2 mA).

Table 44 - Set Input Filter

Bits				Channel	
03	02	01	00	Input Channel 0	
07	06	05	04	Input Channel 1	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200 Hz	No low pass
0	0	0	1	1200 Hz	100 ms low pass
0	0	1	0	1200 Hz	500 ms low pass
0	0	1	1	1200 Hz	1000 ms low pass
0	1	0	0	600 Hz	No low pass
0	1	0	1	600 Hz	100 ms low pass
0	1	1	0	600 Hz	500 ms low pass
0	1	1	1	600 Hz	1000 ms low pass
1	0	0	0	300 Hz	No low pass
1	0	0	1	300 Hz	100 ms low pass
1	0	1	0	300 Hz	500 ms low pass
1	0	1	1	300 Hz	1000 ms low pass
1	1	0	0	150 Hz	No low pass
1	1	0	1	150 Hz	100 ms low pass
1	1	1	0	150 Hz	500 ms low pass
1	1	1	1	150 Hz	1000 ms low pass

Table 45 - Configure Your Outputs for the 1794-IF2XOF2I Analog Combo Module

Configuration Bits				Nominal Range	Data Type	Output Values[1]		Update Rate
MSD		LSD				Hexadecimal	Decimal	
0	0	0	1	4...20 mA	Signed 2's complement	<0000...7878>	<0000...30840>	5.0 ms
0	0	1	0	±10V	Signed 2's complement	<8618...79E8>	<-31208...31208>	2.5 ms
0	0	1	1	±5V	Signed 2's complement	<8618...79E8>	<-31208...31208>	2.5 ms
0	1	0	0	0...20 mA	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	0	1	4...20 mA	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	1	0	0...10V	Signed 2's complement %	<0...2710>	<0...10000>	5.0 ms
0	1	1	1	±10V	Signed 2's complement %	<D8F0...2710>	<-10000...10000>	5.0 ms
1	0	0	0	0...20 mA	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	0	1	4...20 mA	Binary	<0000...F0F1>	<0000...61681>	5.0 ms
1	0	1	0	0...10V	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	0	1	1	0...5V	Binary	<0000...F3CF>	<0000...62415>	2.5 ms
1	1	0	0	0...20 mA	Offset binary	<8000...F9E8>	<32768...63976>	2.5 ms
1	1	0	1	4...20 mA	Offset binary	<8000...F878>	<32768...63608>	5.0 ms
1	1	1	0	±10V	Offset binary	<0618...F9E8>	<1560...63976>	2.5 ms
1	1	1	1	±5V	Offset binary	<0618...F9E8>	<1560...63976>	2.5 ms

(1) < and > indicate the overrun beyond the actual range (about 5%).

Notes:

Calibrate Your Module

When and How to Calibrate Your Isolated Analog Module

Your module is shipped to you already calibrated for 150 Hz, 300 Hz, and 600 Hz. If you are checking calibration, or if it becomes necessary to recalibrate the module, you must do so with the module in a FLEX I/O system. The module must communicate with the processor and industrial terminal.

Before calibrating the module, if ladder logic is used for calibration rather than the GUI available for the 1794-IF4I and 1794-IF2XOF2I modules, you must enter ladder logic into the processor memory, so that you can initiate BTWs to the module, and the processor can read inputs from the module.

Periodically (frequency based on your application), check your module calibration. Calibration may be required to remove module error due to aging of components in your system.

Calibration can be accomplished using any of three methods:

- Manual calibration, described as follows:
- 6200 I/O CONFIGURATION software – See your 6200 software publications for procedures for calibrating.
- Studio 5000 Logix Designer application GUI available for the IF2XOF2I and IF4I with an EtherNet/IP or ControlNet adapter. Studio 5000 Logix Designer application guides the user through the process sequentially with no need for use of block transfers.

When calibrating your module, you must perform:

- Input and output module (in voltage mode) – Offset calibration first, gain calibration second.
- Output module (in current mode) – Gain calibration first, offset calibration second, and another gain calibration third.

Tools and Equipment

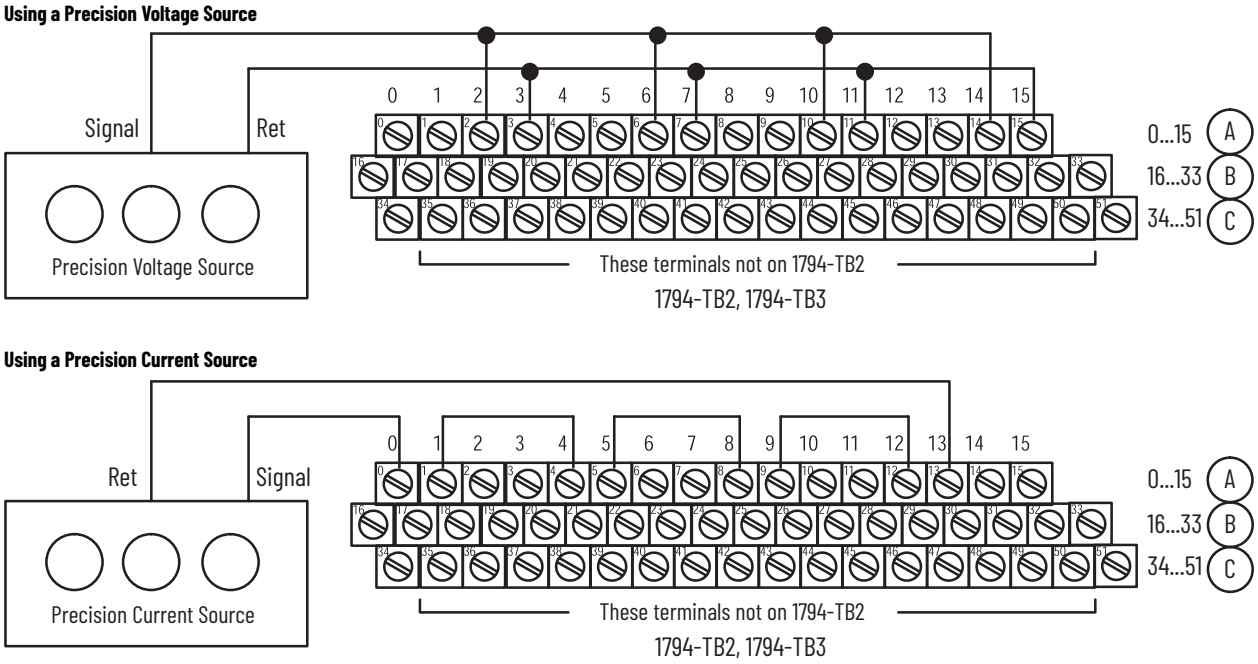
To calibrate your input module, you need the following tools and equipment.

Table 46 - Tools for Calibration

Tool or Equipment	Description	Model/Type	Available from:
Precision Voltage/Current Source	0...10.25V, 10 µV resolution or better 0...21 mA, 100 nA or better	HP3245A or equivalent	–
Precision Voltage/Current Meter	0...10.5V, 10 µV or better 0...22 mA, 100 nA or better	Datron, Wavetek or equivalent	–
Industrial Terminal and Interconnect Cable	Programming terminal for Allen-Bradley family processors	Catalog numbers 1770-T3 or 1784-T45, 1784-T47, 1784-T50...	rockwellautomation.com

ATTENTION: The isolated analog modules are already calibrated for 150 Hz, 300 Hz, and 600 Hz when shipped. No recalibration is required when switching between these conversion rates.

Figure 13 - Calibration Set-up



Calibrate Your Isolated Analog Input Module

The analog input module is already calibrated for 150 Hz, 300 Hz, and 600 Hz when shipped. No recalibration is required when switching between these conversion rates. Recalibration is required when going to 1200 Hz conversion rate. Calibration of the module consists of applying a voltage or current across each input channel for offset and gain calibration.

Bits Used During Calibration

See Chapter 4 for bit/word descriptions. The following bits are used during calibration of your module:

IC = initiate configuration. This bit must be set (1) to initiate calibration.

RV = revert to defaults. When this bit is set (1) during a calibration sequence, the default values for the selected channels are used for the calibration coefficients. This bit normally reset (0).

QK = quick calibration. When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. For example, if a calibration is performed in a voltage mode, QK allows the calibration coefficient to be stored to all voltage modes. This bit is normally reset (0).

CK = calibration clock. When this bit is set to 1, calibration mode starts and calibration coefficients for the selected channels are accepted. When cleared to 0, the accepted current calibration coefficients are stored to the selected channels, applied, and calibration mode exited. Monitor status bits DN and BD of success of calibration.

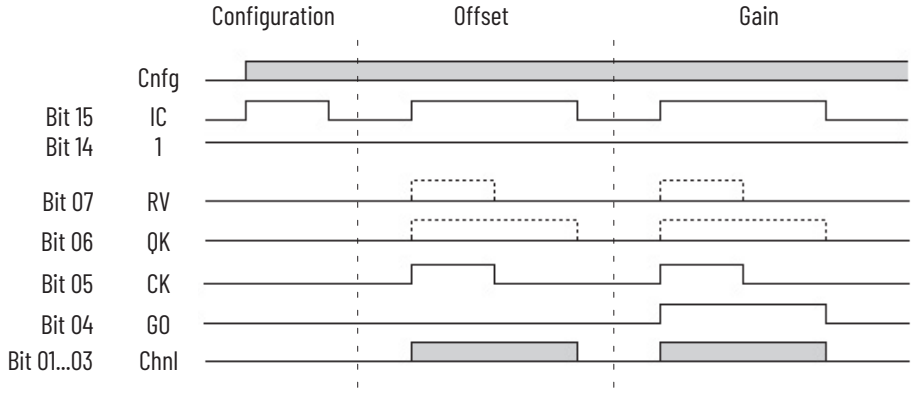
GO = gain/offset select. When this bit is set to 1, a 0 to 1 to 0 transition pattern of the CK bit causes a gain calibration to be performed. When this bit is cleared to 0, a 0 to 1 to 0 transition pattern of the CK bit caused an offset calibration to be performed.

Offset Calibration for Inputs

See the input timing diagram when calibrating the module. Normally all inputs are calibrated together. To calibrate the offset, proceed as follows:

1. The module must be calibrated in an operating system. Connect your module in a calibration setup as shown before.
2. Send a block transfer write (BTW) to the module with individual channel bits set for the configuration desired for each input. This effectively ends any previous configuration of the module/channel.

Figure 14 - Input Calibration Timing Diagram



3. Apply offset voltage (0V) or current (0 mA) to the inputs to be configured.
4. Send a block transfer write to set the IC bit and CK bit (1), and reset the GO bit (0). This tells the module to determine the offset coefficients for the selected channels.

   If you also set the RV bit to 1, the default values are assigned to each channel. The default values are near but not precisely on the calibration mark.
5. Send another BTW to the module to reset the CK bit (0). When the GO bit is low, the previously determined offset coefficients are stored in EEPROM for the selected channels. If QK is set (1) high, the same coefficients are stored to all "like" configurations (for example, if configuration bits are set for a specific voltage, both unipolar/bipolar, x1/x2 – have the same coefficients stored – see Table 47). If calibrated for 0...20 mA current range, 4...20 mA range channels are also automatically calibrated.

Table 47 - Input Calibration Timing Diagram

Configuration	Nominal Range	Data Type	Comments
4	0...20 mA	Signed 2's complement %	If you calibrate any of this group, the rest of the group is also calibrated.
8	0...20 mA	Binary	
C	0...20 mA	Offset binary	
6	0...10V	Signed 2's complement %	If you calibrate any of this group, the rest of the group is also calibrated.
A	0...10V	Binary	
B	0...5V	Binary	
2	±10V	Signed 2's complement	If you calibrate any of this group, the rest of the group is also calibrated.
7	±10V	Signed 2's complement %	
E	±10V	Offset binary	
3	±5V	Signed 2's complement	If you calibrate any of this group, the rest of the group is also calibrated.
F	±5V	Offset binary	
1	4...20 mA	Signed 2's complement	If you calibrate 0...20 mA range, all 4...20 mA range is also calibrated.
5	4...20 mA	Signed 2's complement %	
9	4...20 mA	Binary	
D	4...20 mA	Offset binary	

6. Monitor the module block transfer read word. Clear the IC bit to 0, and offset calibration is ended.

Set the Input Gain

Set the gain of the module second. You must set the offset before setting the gain.

1. Apply gain voltage (5.25V or 10.25V) or current (21.0 mA) to selected inputs.
2. Send a BTW to the module to set the IC bit and the CK bit to 1 and the GO bit to 1. This tells the module to determine the gain voltage/current for the selected channels. If you also set the RV bit to 1, default values are used on all selected channels.
3. Send a BTW to the module to reset the CK bit to 0 with the GO bit still 1. This stores previously determined coefficients into EEPROM on selected channels. If QK is set (1), the same coefficients are stored to all "like" configurations. For example, if the configuration is set to voltage, bipolar/polar, X1/X2 is also configured. See Table 47.
4. Monitor the module block transfer read word. Clear the IC bit. Gain calibration is ended.

Calibrate Your Isolated Analog Output Module

Calibration of the module consists of measuring a voltage or current across each output, and calculating an offset or gain correction value.

IMPORTANT	Voltage calibration requires offset calibration followed by gain calibration. Current calibration requires gain calibration followed by offset calibration, and then a limited gain calibration using corrected coefficients.

Bits Used During Calibration

See Chapter 4 for bit/word descriptions. The following bits are used during calibration of your module:

IC = initiate configuration. This bit must be set (1) to initiate calibration.

RV = revert to defaults. When this bit is set (1) during a calibration sequence, the default values for the selected channels are used for the calibration coefficients. This bit normally reset (0).

QK = quick calibration. When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. For example, if a calibration is performed in a voltage mode, QK allows the calibration coefficient to be stored to all voltage modes.

CK = calibration clock. When this bit is set to 1, calibration mode starts and calibration coefficients for the selected channels are accepted. When cleared to 0, the accepted current calibration coefficients are stored to the selected channels, applied, and calibration mode exited. Monitor status bits DN and BD of success of calibration.

GO = gain/offset select. When this bit is set to 1, a 0 to 1 to 0 transition pattern of the CK bit causes a gain calibration to be performed. When this bit is cleared to 0, a 0 to 1 to 0 transition pattern of the CK bit caused an offset calibration to be performed.

Calibrate Voltage Outputs

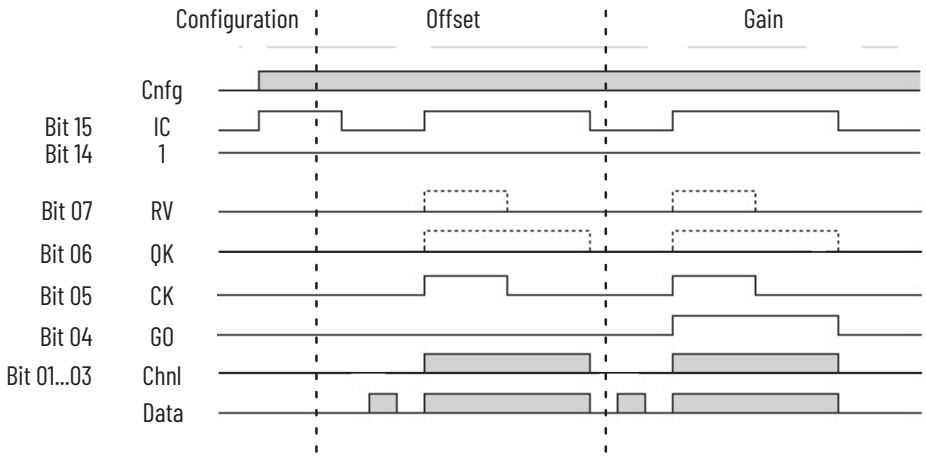
Voltage calibration requires offset calibration followed by gain calibration.

Offset Calibration for Voltage Outputs

See the output timing diagram when calibrating the module. Normally all outputs are calibrated together. To calibrate the offset of an output, proceed as follows:

1. If you are not calibrating all channels with the same configuration, select the channel to be calibrated by setting the bit for that channel.
2. Send a block transfer write (BTW) to the module with individual channel bits set for the configuration desired for each output. This effectively ends any previous configuration of the module/channel.

Figure 15 - Output Calibration Timing Diagram



3. Clear all offset and gain coefficients by:
   a. Set output data to 0 and the IC bit to 1
   b. With GO = 0, toggle the CK bit
   c. With GO = 1, toggle the CK bit
   d. Clear the IC bit
4. Send a block transfer write with the output values for offset voltage to the module; -31208 for -10V mode 2. Measure the output.

   Calculate the offset correction for each channel:

   offset_corr = (-10V – measured_value) X 3120.7619
5. Enter these offset corrections in the output word for each channel being calibrated.
6. Send a block transfer write with the IC bit and the CK bit set to 1. With GO low (0), the module copies the "offset_corr" coefficients (signed 2's complement format) from the data words into offset storage for the selected channels. If you set RV high (1), the default values are copied to all channels.
7. With a BTW, reset the CK bit (0). With the GO bit low (0), the previously determined offset coefficients are stored in EEPROM for the selected channel.
8. Monitor the block transfer read. Clear the IC bit to 0. Offset calibration is completed.

Gain Calibration for Outputs

1. Send a block transfer write to the module to set the output values for gain voltage; +31208 for +10V mode 2. Measure the output.

   Calculate the gain correction for each channel as follows:

   gain_corr = (+10V – measured_value) X 3276.76
2. Enter these gain corrections in the output word for each channel being calibrated.
3. Send a block transfer write with the CK bit set to 1. With GO high, the module copies "gain_corr" coefficients (signed 2's complement format) from the data words into gain storage for the selected channels. If RV is high, default values are copied to all channels.
4. Send a block transfer write with CK set to 0. With GO high, the previously determined gain coefficients are stored into EEPROM as directed by the channel selection.
5. Clear the IC bit to 0. Gain calibration is ended.

Calibrate Current Outputs

Current calibration requires gain calibration followed by offset calibration, and a limited gain calibration using corrected coefficients.

Gain Calibration for Current Outputs

1. Send a block transfer write to the module to set the output values for gain voltage; F3CF hex for 20.0 mA mode 8. Measure the output.

   Calculate the gain correction for each channel as follows:

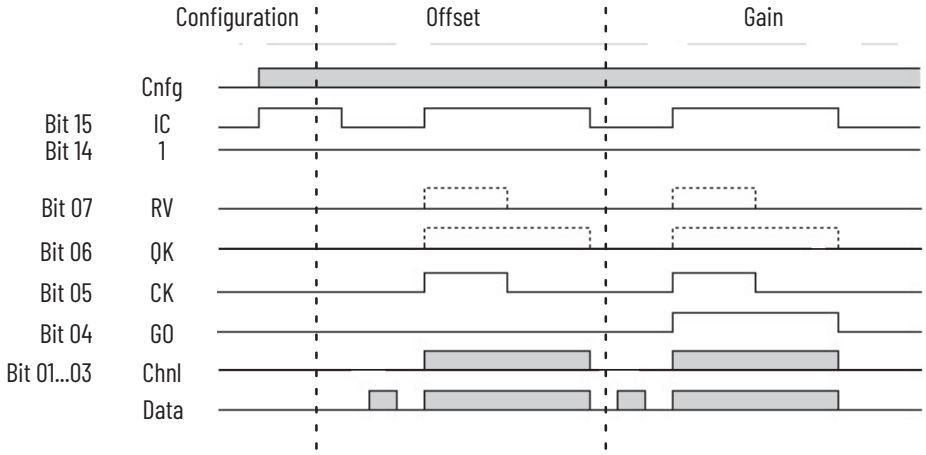
   gain_corr = (0.02 A – measured_value) X 3202194.613
2. Enter these gain corrections in the output word for each channel being calibrated. Record each of the values to be used later.
3. Send a block transfer write with the CK bit set to 1. With GO high, the module copies "gain_corr" coefficients (signed 2's complement format) from the data words into gain storage for the selected channels. If RV is high, default values are copied to all channels.
4. Send a block transfer write with CK set to 0. With GO high, the previously determined gain coefficients are stored into EEPROM as directed by the channel selection.
5. Clear the IC bit to 0. Gain calibration is ended.

Offset Calibration for Current Outputs

See the output timing diagram when calibrating the module. Normally all outputs are calibrated together. To calibrate the offset of an output, proceed as follows:

1. If you are not calibrating all channels with the same configuration, select the channel to be calibrated by setting the bit for that channel.
2. Send a block transfer write (BTW) to the module with individual channel bits set for the configuration desired for each output. This effectively ends any previous configuration of the module/channel.

Figure 16 - Output Calibration Timing Diagram



3. Clear all offset and gain coefficients by:
   a. Set output data to 0 and the IC bit to 1
   b. With GO = 0, toggle the CK bit
   c. With GO = 1, toggle the CK bit
   d. Clear the IC bit
4. Send a block transfer write with the output values for offset voltage to the module; +1560 for 0.5 mA mode 8. Measure the output.

   Calculate the offset correction for each channel as follows:

   offset_corr = (0.0005 – measured_value) X 1524873.192

5. Enter these offset corrections in the output word for each channel being calibrated. Record each of the values to be used later.
6. Send a block transfer write with the IC bit and the CK bit set to 1. With GO low (0), the module copies the "offset_corr" coefficients (signed 2's complement format) from the data words into offset storage for the selected channels. If you set RV high (1), the default values are copied to all channels.
7. With a BTW, reset the CK bit (0). With the GO bit low (0), the previously determined offset coefficients are stored in EEPROM for the selected channel.
8. Monitor the block transfer read. Clear the IC bit to 0. Offset calibration is completed. Proceed with final gain calibration.

Final Gain Calibration for Current Inputs

After performing a gain calibration and an offset calibration:

1. Enter a new gain correction calculated as follows into the respective output words:

   new gain_corr = gain_corr – (2 x offset_corr)
2. Send a block transfer write with the CK bit set to 1. With GO high, the module copies "gain_corr" coefficients (signed 2's complement format) from the data words into gain storage for the selected channels. If RV is high, default values are copied to all channels.
3. Send a block transfer write with CK set to 0. With GO high, the previously determined gain coefficients are stored into EEPROM as directed by the channel selection.
4. Clear the IC bit to 0. Gain calibration is ended.

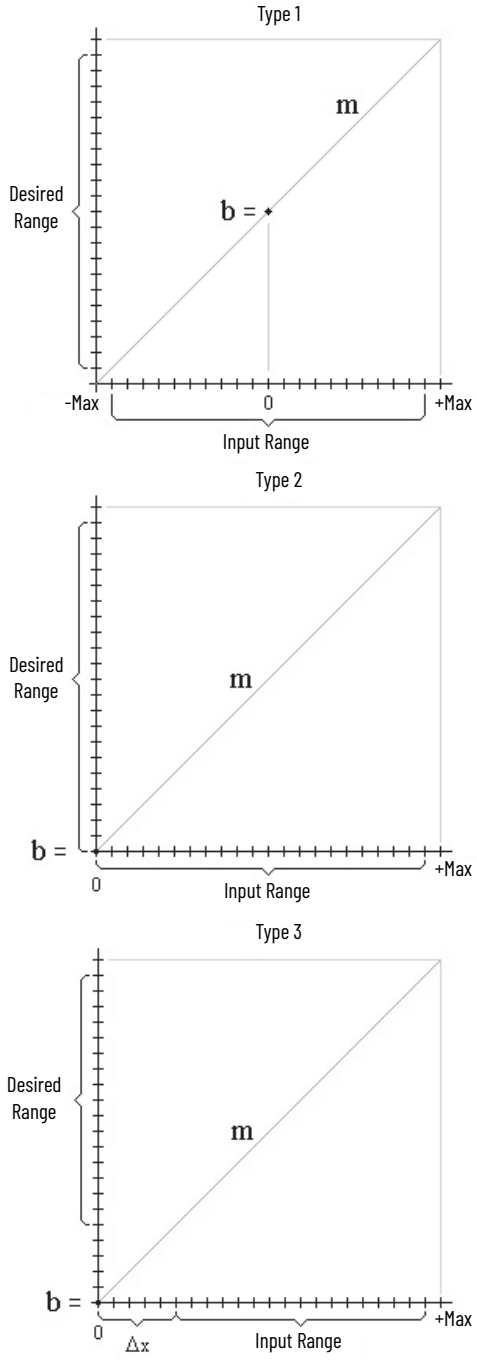
Scaling Inputs

Inputs are scaled using the *y = mx + b* linear formula, as illustrated by the three types as shown.

Configuration	Nominal Range	Data Type	Scale Figure	Output Range	ΔX
1	4...20 mA	Signed 2's complement	Type 2	30840	NA
2	±10V	Signed 2's complement	Type 1	63938	NA
3	±5V	Signed 2's complement	Type 1	62416	NA
4	0...20V	Signed 2's complement %	Type 2	10000	NA
5	4...20 mA	Signed 2's complement %	Type 2	10000	NA
6	0...10V	Signed 2's complement %	Type 2	10000	NA
7	±10V	Signed 2's complement %	Type 1	20000	NA
8	0...20 mA	Binary	Type 2	62415	NA
9	4...20 mA	Binary	Type 2	61681	NA
A	0...10V	Binary	Type 2	63938	NA
B	0...5V	Binary	Type 2	62415	NA
C	0...20 mA	Offset binary	Type 3	62416	1560
D	4...20 mA	Offset binary	Type 3	30840	32768
E	±10V	Offset binary	Type 3	63938	799
F	±5V	Offset binary	Type 3	62416	1560

The gain, m, and offset, b, coefficients are calculated as follows:

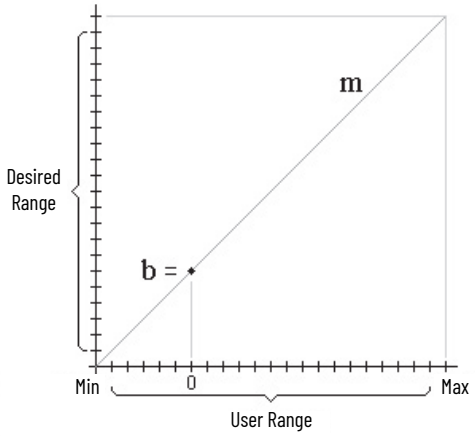
m = Desired Range/Input Range
b = Desired value when input returns zero (Type 1 and Type 2)
b = – m(Δx) + (bottom of Desired Range) (Type 3)



Scaling Outputs

Outputs are scaled in the same manner as the inputs as shown in the following illustration.

Configuration	Nominal Range	Data Type	Output Range	Z
1	4...20 mA	Signed 2's complement	30840	0
2	±10V	Signed 2's complement	62416	0
3	±5V	Signed 2's complement	62416	0
4	0...20V	Signed 2's complement %	10000	0
5	4...20 mA	Signed 2's complement %	10000	0
6	0...10V	Signed 2's complement %	10000	0
7	±10V	Signed 2's complement %	20000	0
8	0...20 mA	Binary	62415	0
9	4...20 mA	Binary	61681	0
A	0...10V	Binary	62415	0
B	0...5V	Binary	62415	0
C	0...20 mA	Offset binary	31208	32768
D	4...20 mA	Offset binary	30840	32768
E	±10V	Offset binary	62416	32768
F	±5V	Offset binary	62416	32768



The gain, m, and offset, b, coefficients are calculated as follows:

m = Output Range/User Range
b = Z – mx

where: Z is the value, from the table that sends a "zero" output[(a)]. x0 is the user signal that is associated with "zero" output.

(a) in 4...20 mA modes, "zero" is 4 mA.

Notes:

Filter Response Conversion

Filter Response for 150 Hz, 300 Hz, and 600 Hz Conversion

Figure 17 - Filter Response at 150 Hz Conversion

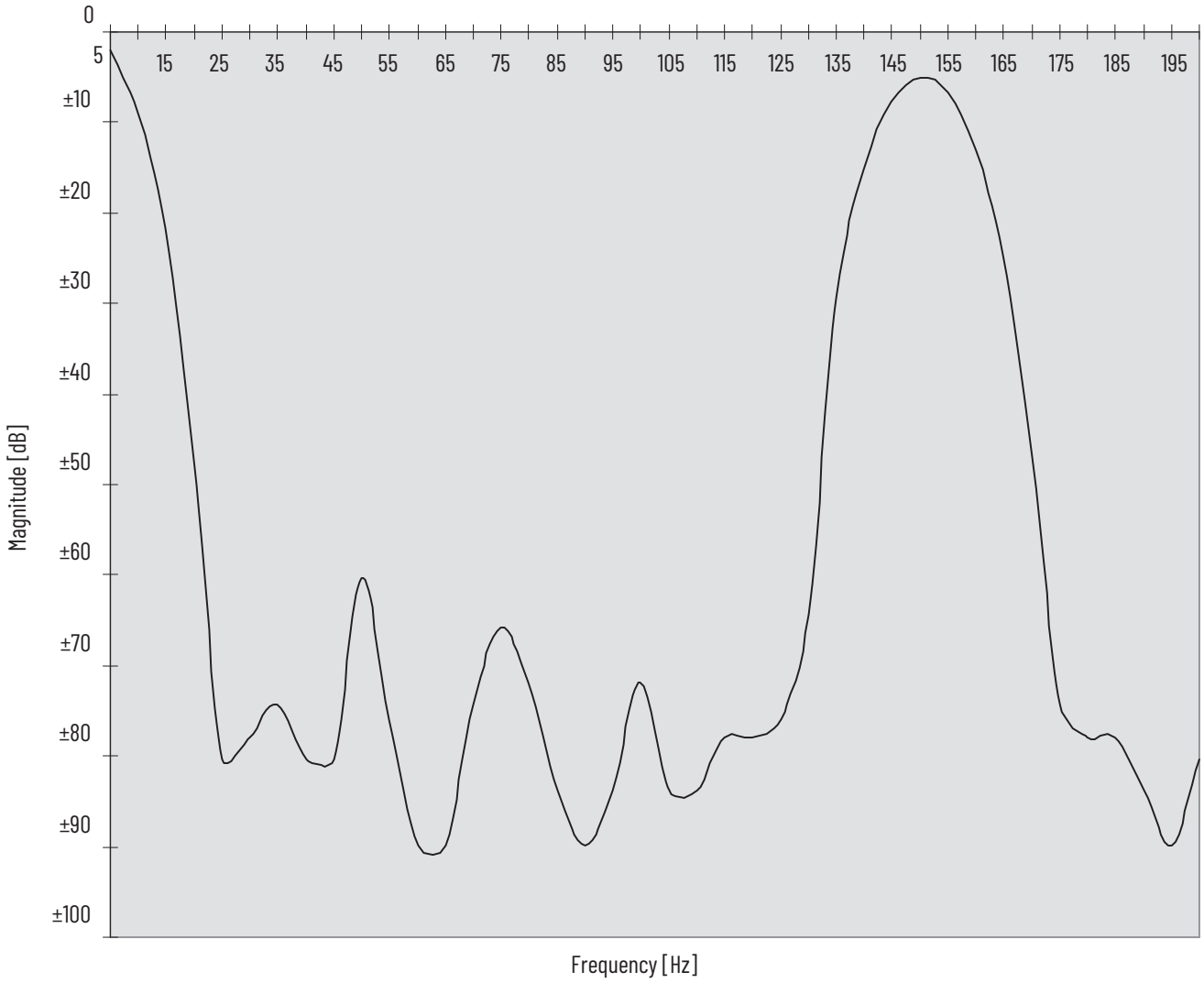


Figure 18 - Filter Response at 300 Hz Conversion

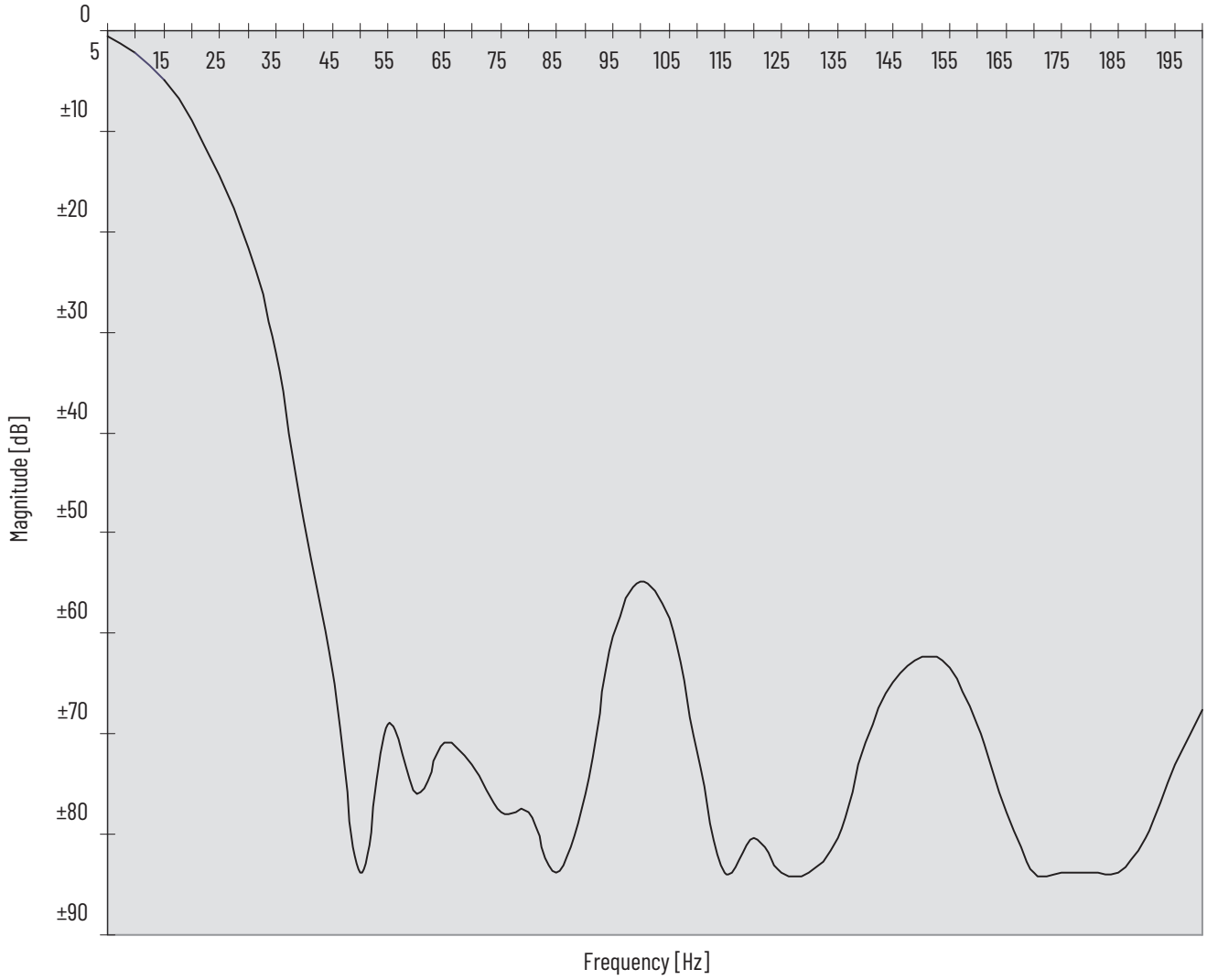
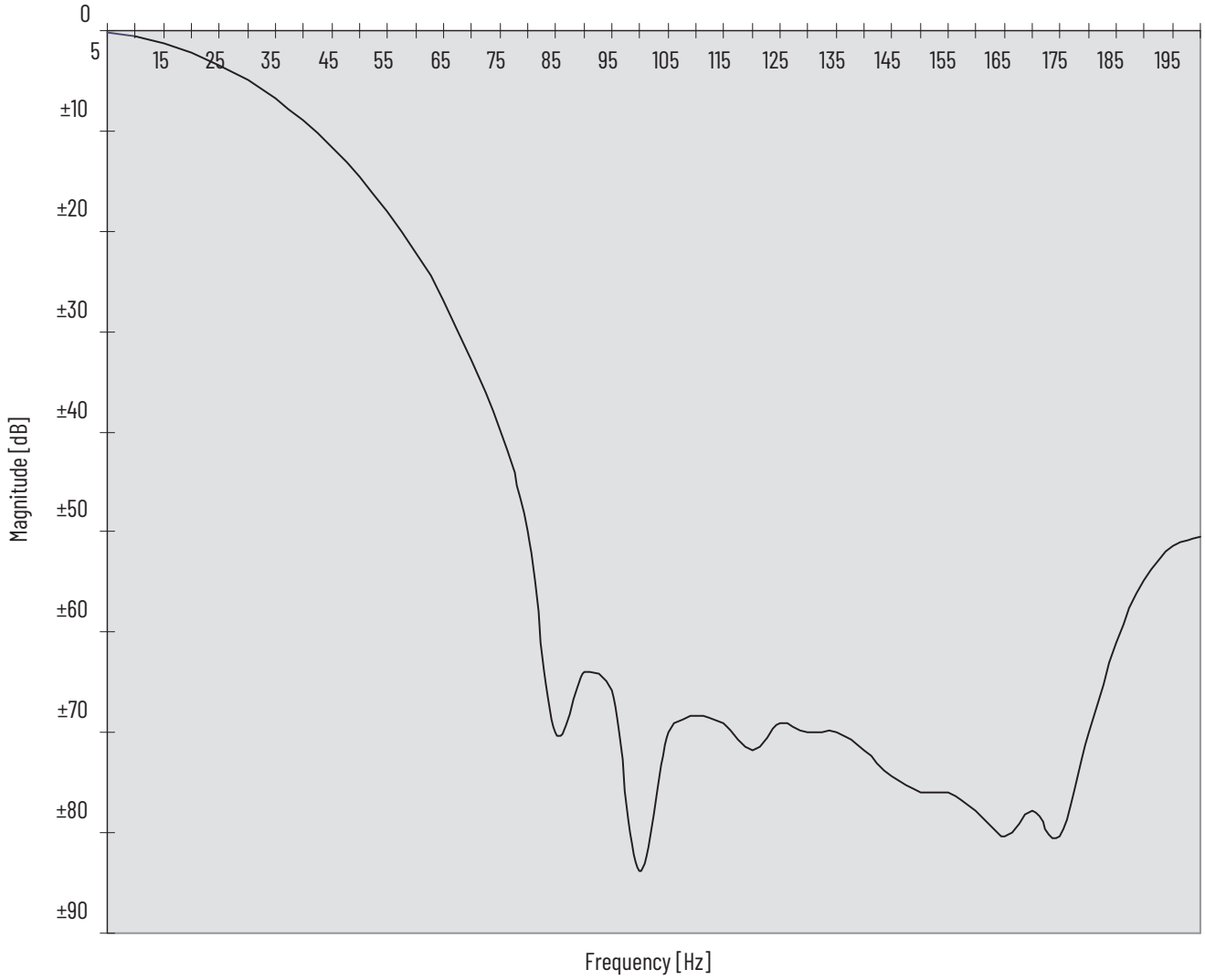


Figure 19 - Filter Response at 600 Hz Conversion



Notes:

Rockwell Automation Support

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Literature Library	Find installation instructions, manuals, brochures, and technical data publications.	rok.auto/literature
Product Compatibility and Download Center (PCDC)	Download firmware, associated files (such as AOP, EDS, and DTM), and access product release notes.	rok.auto/pcdc

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Publication 1794-UM008F-EN-P - November 2023
Supersedes Publication 1794-UM008E-EN-P - March 2020

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